IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

VOLTERRA SEMICONDUCTOR LLC, Plaintiff, v. MONOLITHIC POWER SYSTEMS, INC., Defendant.	))))))))))	Redacted: Public Version C.A. No. 19-2240-CFC [redacted]

DECLARATION OF SARIA TSENG IN SUPPORT OF DEFENDANT MONOLITHIC POWER SYSTEMS'S MOTION TO DISQUALIFY FISH & RICHARDSON P.C.

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Dated: April 30, 2020

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

VOLTERRA SEMICONDUCTOR LLC, *Plaintiff,* v. MONOLITHIC POWER SYSTEMS, INC., *Defendant.*	)	C.A. No. 19-02240-CFC **CONFIDENTIAL—FILED UNDER SEAL PURSUANT TO LR 26.2**

DECLARATION OF SARIA TSENG IN SUPPORT OF DEFENDANT MONOLITHIC POWER SYSTEMS'S MOTION TO DISQUALIFY FISH & RICHARDSON P.C.

1. I, Saria Tseng, am the Vice President of Strategic Corporate Development, General Counsel & Corporate Secretary for Monolithic Power Systems, Inc. ("MPS"). I have been employed by MPS as General Counsel since late 2004. In my role as General Counsel of MPS, among other responsibilities I oversee all MPS's legal affairs and retain and supervise its outside counsel. I provide this declaration based on my personal knowledge and on behalf of MPS.

I. Overview of MPS's Relationship with Fish

2. MPS is a leading semiconductor company that designs, develops, and markets high-performance power solutions. MPS's core strengths include deep system-level and applications knowledge, strong analog design expertise and

innovative proprietary process technologies. These combined strengths enable MPS to deliver highly integrated monolithic products that offer energy efficient, cost-effective, easy-to-use solutions for power systems found in computing and storage, automotive, industrial, communications and consumer applications. One of MPS's missions is to improve efficiency and reduce total energy consumption in its customers' systems with green, practical, and compact solutions. This mission has manifested in the development of many different models and components of efficient power solutions, including the accused 48V-1V Power Solution for CPU, SoC, or ASIC Controller.

3. In order to protect its innovations and proprietary technology advantage and maintain its competitive position in the power solution space, MPS set out to retain a law firm to guide MPS and to help develop its IP portfolio, IP litigation and business strategies. Fish & Richardson ("Fish") made a presentation to MPS, claiming that they were the best and most recognizable intellectual property law firm in the country, with more expertise in the electrical engineering area than other law firms in the country. Fish was retained to not only represent MPS in a "bet the company lawsuit" at the ITC and subsequently several other litigation matters, but also was retained as the primary outside general counsel to guide and help develop our IP portfolio, IP litigation and business strategies for a wide range of matters. To fully execute the engagement with Fish, over a five year

period, MPS was encouraged to disclose and did disclose to Fish attorneys its most strategic, sensitive and confidential know-how and business aspirations so that Fish could most effectively develop MPS's IP portfolio, litigation and business strategies. MPS is distressed that this same firm now is exploiting the same know-how and strategic information, which was entrusted to Fish in confidence by MPS, in the present lawsuit being brought against MPS.

4. MPS had a long and productive relationship with Fish, from 2007 to 2012. Fish's representation of MPS focused on advice, litigation, and patent prosecution, all of which were related to power solutions including at least DC-to-DC power converters; the subject matter in the present case. Fish's representation was far reaching and touched every aspect of MPS's business. Fish acted as MPS's IP general counsel. When MPS learned that Fish, our former counsel for patent matters related to power solutions, was suing us now for patent infringement on Volterra's behalf on the same subject matter, we felt Fish had betrayed the trust we placed in it. If Fish is allowed to continue to represent Volterra in the present lawsuit, MPS is gravely concerned that the confidential know how and business information MPS gave to Fish in confidence was used and will continue to be used against MPS.

5. I understand that Volterra accuses MPS's 48V-1V Power Solution for CPU, SoC, or ASIC Controller in this case. This product is an example of a DC-to-

DC converter and its development was announced last year. It is just now coming to market and builds on MPS' decades of experience designing DC-to-DC converters and the components they are constructed from. Fish's representation of MPS certainly included detailed investigations and disclosure of information regarding MPS's DC-to-DC converter technologies, as well as MPS's related patents and trade secrets and strategies for protecting this intellectual property. MPS was encouraged to and did reveal this information to Fish with the understanding that it would be protected by the attorney-client privilege and never used against MPS.

6. I understand that our accounting manager, Alistair Burton, has submitted a declaration authenticating [redacted] invoices Fish issued to us over the course of our relationship, from 2007 to 2012. I understand that his declaration has identified the invoices as Exhibit 1. I am also familiar with these invoices and the matters which they describe and will refer to these invoices and matters below. To the best of my recollection, all the invoices were settled, and there were no unresolved disputes.

7. Attached as Exhibit 2 is a true and correct copy of a letter entitled "Attorney-Client Engagement of Fish & Richardson P.C." [redacted]

8. [redacted]

9. Attached as Exhibit 3 is a true and correct copy of two related letters [redacted]

10. [redacted]

[redacted]

11. [redacted]

12. Attached as Exhibit 4 is a true and correct copy of a letter entitled "Formalizing the end of our Attorney/Client Relationship; Request for File Disposition Instructions." [redacted]

[redacted]

13. [redacted]

14. I understand that our accounting manager, Alistair Burton, has submitted a declaration in which he provides analytics for 13 different matters Fish worked on. Each of these thirteen matters can be grouped into three general areas of representation, advice, litigation, and patent prosecution. I provide further details about each of these matters grouped into these three categories below.

II. Fish's Representations Advising MPS on Patent Issues for DC-to-DC Converter Technologies

15. [redacted]

[redacted]

16. [redacted]

[redacted]

17. [redacted]

[redacted]

18. [redacted]

[redacted]

[redacted]

19. [redacted]

20. [redacted]

21. [redacted]

22. [redacted]

23. [redacted]

24. [redacted]

25. [redacted]

26. [redacted]

27. [redacted]

28. [redacted]

29. [redacted]

[redacted]

30. [redacted]

31. [redacted]

[redacted]

32. [redacted]

33. [redacted]

34. [redacted]

III. Fish's Representations of MPS in Patent Litigation for Related Technologies

35. Fish did not just provide MPS legal advice on MPS's patent portfolio and products. Fish also represented MPS in several patent litigations and planned litigations, as both a plaintiff and defendant.

36. In fact, during the course of Fish's relationship with MPS, from 2007 to 2012, Fish represented MPS in *all* MPS's patent litigation matters in some capacity. As such, all these previous litigations involved infringement and validity issues, concerning power solutions and converters and the related legal issues in this case.

37. While these previous ligations did not involve Volterra, these previous litigations did involve competitors of MPS and Volterra, and the technologies involved all relate to power supplies and converters implicated by Volterra's asserted claims against MPS. Thus, I expect Volterra (through Fish) to seek discovery into many of the same products and facts that were at issue in those prior cases.

38. Further, if Fish is allowed to remain Volterra's counsel in this case, presumably they will seek to cross examine our employees, including potentially many of the same employees Fish worked with on these prior matters. Fish, through those matters, will be able to exploit its knowledge of these witnesses 'demeanor, prior deposition and witness training, knowledge, experiences, weaknesses, and insecurities in conducting these depositions and cross examinations. A deposition or cross examination is not a comfortable scenario to begin with: that stress is exponentially higher when the counsel grilling the witness is someone the witness knows and worked with before. This is particularly

worrisome as Fish has still not named the specific attorneys and staff whom Fish are now screening from the case, and MPS cannot know what knowledge passed in the years before this wall was put in place.

39. [redacted] As an example, Fish's representation of MPS in *Monolithic Power Systems Inc. v. v. Silergy Corporation,* No. 2:10-cv-01533-CAS-AGR (C.D. Cal, filed on Mar. 02, 2010) ("MPS v. Silergy") was billed under this number. A true and correct copy of the complaint from this case is attached as Exhibit 7. This complaint alleged infringement of the aforementioned '643 patent, which is related to DC-DC power converter technologies, as discussed above.

40. Attached as Exhibit 8 is also a true and correct copy of the first amended complaint in the MPS v. Silergy case, filed on September 21, 2010. In it, MPS further alleged infringement of USP 7,714,558, which is entitled "Short circuit current ratcheting in switch mode DC/DC voltage regulators." This patent is also related to DC-to-DC converters like the one implicated by Volterra's allegations here.

41. The MPS v. Silergy litigation was not the only case where Fish asserted the '643 patent on MPS's behalf. Fish also asserted it against Chip

Advanced Technology Inc., [redacted] in *Monolithic Power Systems Inc. v. Chip Advanced Technology Inc.*, No. 2:07-cv-08065-VBF-VBK (C.D. Cal., filed on Dec. 11, 2007) ("MPS v. CAT"). Attached as Exhibit 9 is a true and correct copy of the complaint from this matter, filed December 11, 2007.

42. [redacted]

43. [redacted]

44. [redacted]

45. Fish did not just represent MPS in asserting its patent portfolio against infringers. Fish also defended MPS from allegations of infringement by others, such as O2 Micro, regarding MPS's power inverter controller products.

46. Attached as Exhibit 10 is a true and correct copy of the complaint for *Monolithic Power Systems Inc. v. O2Micro International Ltd.*, No. 4:08-cv-04567-CW (N.D. Cal., filed on Oct. 01, 2008) ("MPS v. O2Micro"), filed on October 1, 2008. MPS sought a declaratory judgement of noninfringement and invalidity of four patents, which are each attached to the complaint exhibits, related to MPS's "power inverter controller products." Fish also represented MPS in an ITC investigation adverse to O2Micro, regarding the same technologies, *Certain Cold Cathode Fluorescent Lamp Inverter Circuits and Products Containing Same*, ITC-337-TA-666 (complaint filed December 15, 2008). Included as Exhibit 11 is a true and correct copy of the complaint for this matter, filed December 15, 2008.

47. The technology involved in the *O2 Micro* case involved power inverters. A power inverter converts DC power to AC power and involves many of the same underlying technologies as DC-to-DC converters, e.g., a power storage device and an energy transfer device. Modern high energy power converters for both DC-to-DC as well as AC-to-DC purposes also often use semiconductors such as MOSFETS as switches that help improve the efficiency of the device by lowering interfering noise or to act as a power control. [redacted]

[redacted]

Thus, Fish's investigation into MPS's products and development of MPS's noninfringement and invalidity positions for the O2 Micro matters are also related to the technology at issue in this case.

48. [redacted] Fish represented Powertech in litigation against O2Micro, in *Powertech Association LLC v. O2Micro International Ltd. et al*, No. 1:09-cv-03446-CW (E.D.N.Y., filed on Aug. 7, 2009) ("Powertech v. O2Micro").

49. Included as Exhibit 12 is a true and correct copy of the complaint for this matter, filed August 7, 2009. In this case, Powertech (through Fish) asserted infringement of three patents: USP 6,979,959, USP 7,279,852, and USP 7,411,360, each entitled "Apparatus and method for striking a fluorescent lamp." The infringement allegations were directed to, among other things "inverter controllers" and "inverter circuit board[s]." As discussed above an inverter converts DC power to AC power, and includes technologies related to DC-DC converters.

50. [redacted]

51. This summary makes clear that Fish's representation of MPS in patent litigation was comprehensive and critical to MPS's core business and technology. Now Fish is attacking MPS at that same core business and technology space. Moreover, the invasive nature of U.S. discovery and litigation is well-known. To represent MPS in all these cases, Fish became intwined in MPS's daily operations, and gained the trust of several key employees. Fish stress tested these employees attempting to identify flaws an opposing counsel could exploit in each witness. Fish encouraged and received cooperation and candid responses during all of it mock-examinations exercises by promising it would protect these confidences through a sacrosanct relationship, the attorney-client privilege. I expect many of

the same witnesses that Fish worked with before during these exercises will be witnesses in this action. Accordingly, the harm that Fish's representation of Volterra is causing (and will cause, should Fish continue representing Volterra) to MPS is not limited to the specific information Fish obtained from the company since it also includes surreptitious knowledge obtained about MPS's witnesses that will likely be deposed and cross examined in this case. It is undermining MPS's and the public's faith in the attorney-client relationship and is presenting hurdles for MPS to defend itself in this case, at least because MPS's potential witnesses may not feel comfortable working with and disclosing information to counsel, since that same counsel could turn around and use that information against MPS.

52. Further, I understand from counsel that Fish has now stated they put an ethical wall in place, but only as of January 21, 2020, the date of our current counsel's first letter to them alerting them to this serious conflict. To date, Fish has not named who precisely is being screened by this ethical wall, identifying them only as attorneys and staff who worked on MPS matters. Even with this information, MPS has no assurance that this attorney client privileged information obtained from MPS has not already been shared with the Fish team on this case prior to the ethical wall being put in place, either intentionally or unintentionally. MPS does not know how long Fish conducted its pre-suit investigations of MPS products and other potential considerations. During this critical timeframe, no wall

was in place with the attorneys who worked with MPS in the past. Moreover, to my knowledge, MPS has never received any representation from Fish that appropriate network barriers and walls were put in place to preclude access from any Fish attorneys to electronic data related to MPS confidential documents, work product, and attorney client communications. Nor did MPS receive confirmation that an expungement from the Fish network and attorneys' hard drives of this electronic data ever occurred.

53. Allowing Fish to sue MPS on behalf of a competitor after spending five years in an intimate and extensive attorney-client relationship with MPS representing it in patent litigation matters, obtaining road maps to MPS's business, analyzing all of MPS's patents, products, and technology (including the technology Fish is currently accusing of infringement) and becoming familiar with the key potential witnesses in this case is unfair to MPS. But even setting aside the specific information Fish learned about MPS in this five-year relationship, the appearance that Volterra's counsel has special access to MPS's privileged information sends a bad message to MPS's employees, MPS's customers, the public and to any potential jurors of this action.

IV. Fish's Representations of MPS in Patent Prosecution for Related Technologies

54. In addition to Fish's general IP advice regarding MPS's business and the specific litigation matters identified above in which Fish represented MPS, Fish

also helped MPS procure its patent portfolio and structure protections for MPS's business. Indeed, Fish prosecuted multiple patents for MPS, guiding MPS in the strategy, maintenance, and growth of its patent portfolio. Fish conducted interviews with MPS personnel and inventors, as well as reviews of MPS's developing technology. Three of these matters in particular involved DC-to-DC converter technology such as buck converters, boost converters, and DC/DC switch mode regulators.

55. [redacted]

56. MPS has retained many of the communications where Fish communicated advice and information related to these prosecution matters. Again, due to the highly confidential and privileged nature of this advice, I have not included them as a sealed exhibit, but they are available for *in camera* inspection.

V. Fish's Conduct Attempting to Distance Itself from MPS Illustrate the Conflict Here

57. [redacted]

58. [redacted]

59. [redacted]

60. [redacted]

61. [redacted]

[redacted]

62. [redacted]

63. [redacted]

64. [redacted]

65. [redacted]

[redacted]

66. [redacted]

67. [redacted]

68. [redacted]

[redacted]

69. [redacted]

70. [redacted]

71. [redacted]

72. [redacted]

73. [redacted]

[redacted]

74. [redacted]

[redacted]

VI. Volterra Has Been Contacting MPS Customers Asserting This Case Relates to All of MPS's Products

75. Finally, to the extent Fish or Volterra argue the scope of this case is narrow and that the scope of any "substantial relationship" between this case and Fish's prior representation of MPS should be limited to only the single accused product identified in Volterra's complaint, sales representatives of MPS have

received multiple reports that representatives of Volterra have been contacting MPS customers, asserting or providing the impression that this matter concerns all of MPS's power systems, attempting to paint MPS in a bad light and threaten all of MPS's business. Volterra should not be allowed to represent that this case relates to all of MPS's products to MPS's customers in an effort to stifle competition, while at the same time Fish is representing to this Court it believes this case involves nothing more than the single MPS product identified in the complaint in attempt to narrow down this case for conflicts purposes.

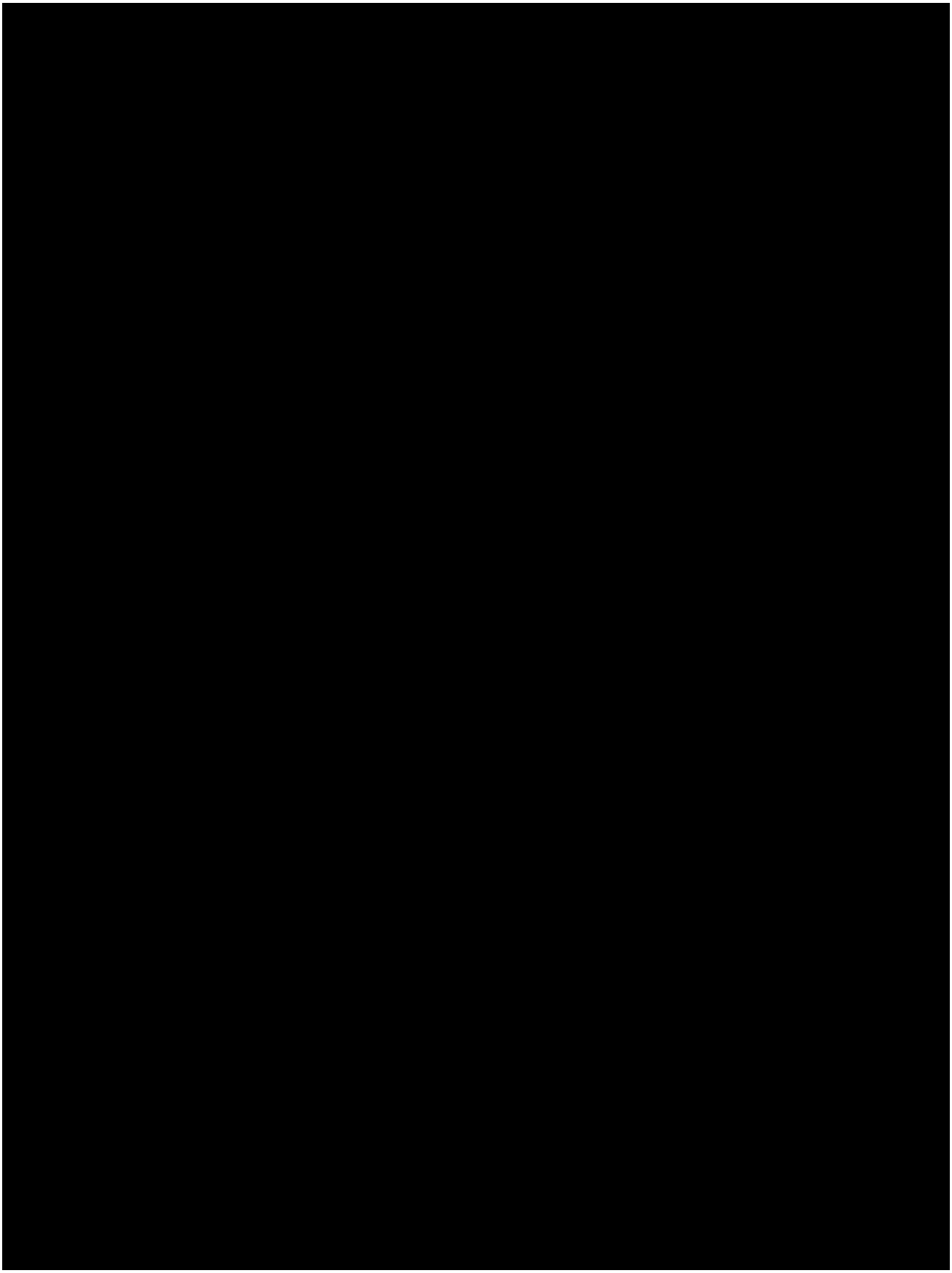
VII. Privileged Materials Relevant to Fish's Conflict Available for *In Camera* Inspection

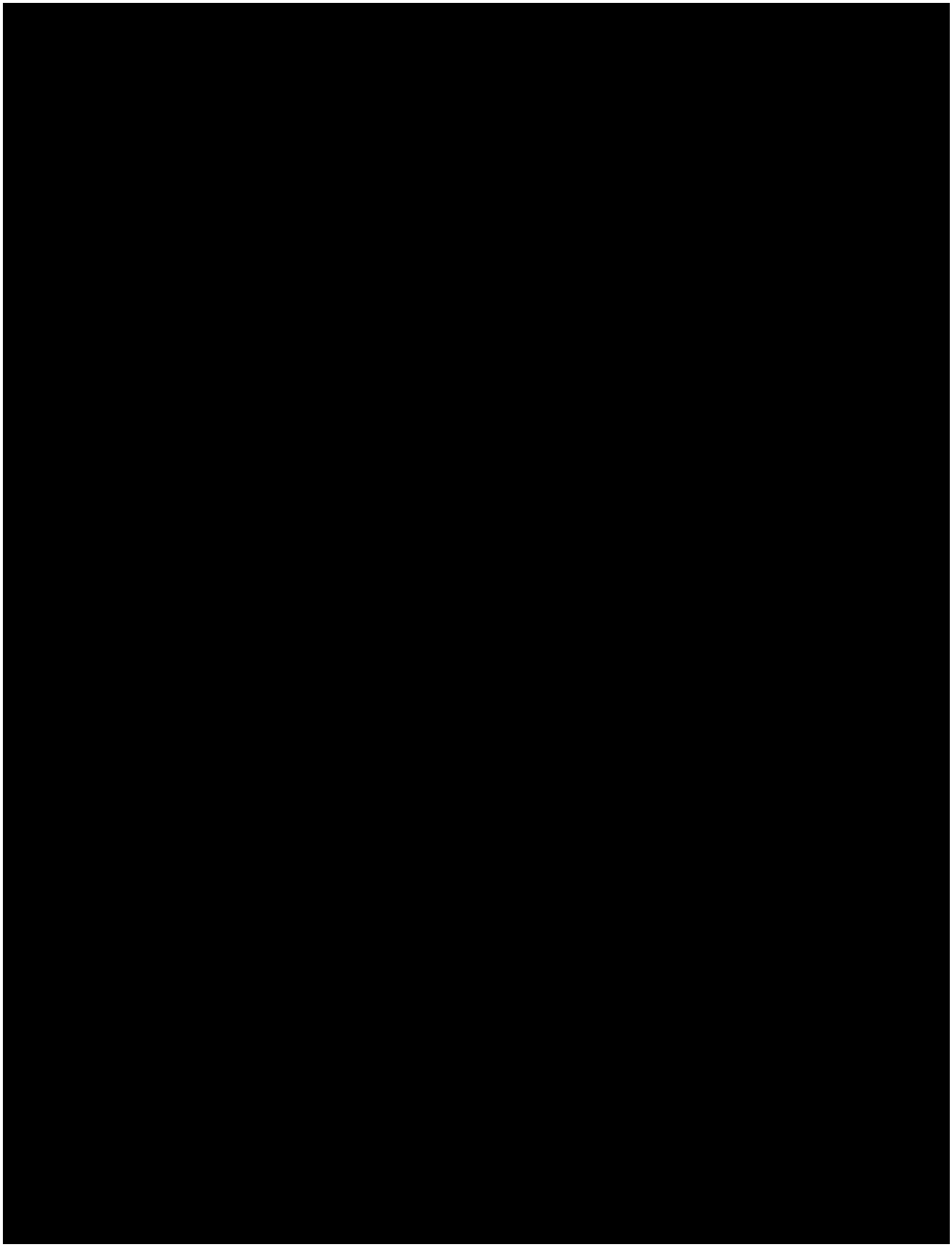
76. As I have identified above, MPS has retained documents and communications which show some of the communications, advice, and information that was at issue in Fish's representation of MPS.

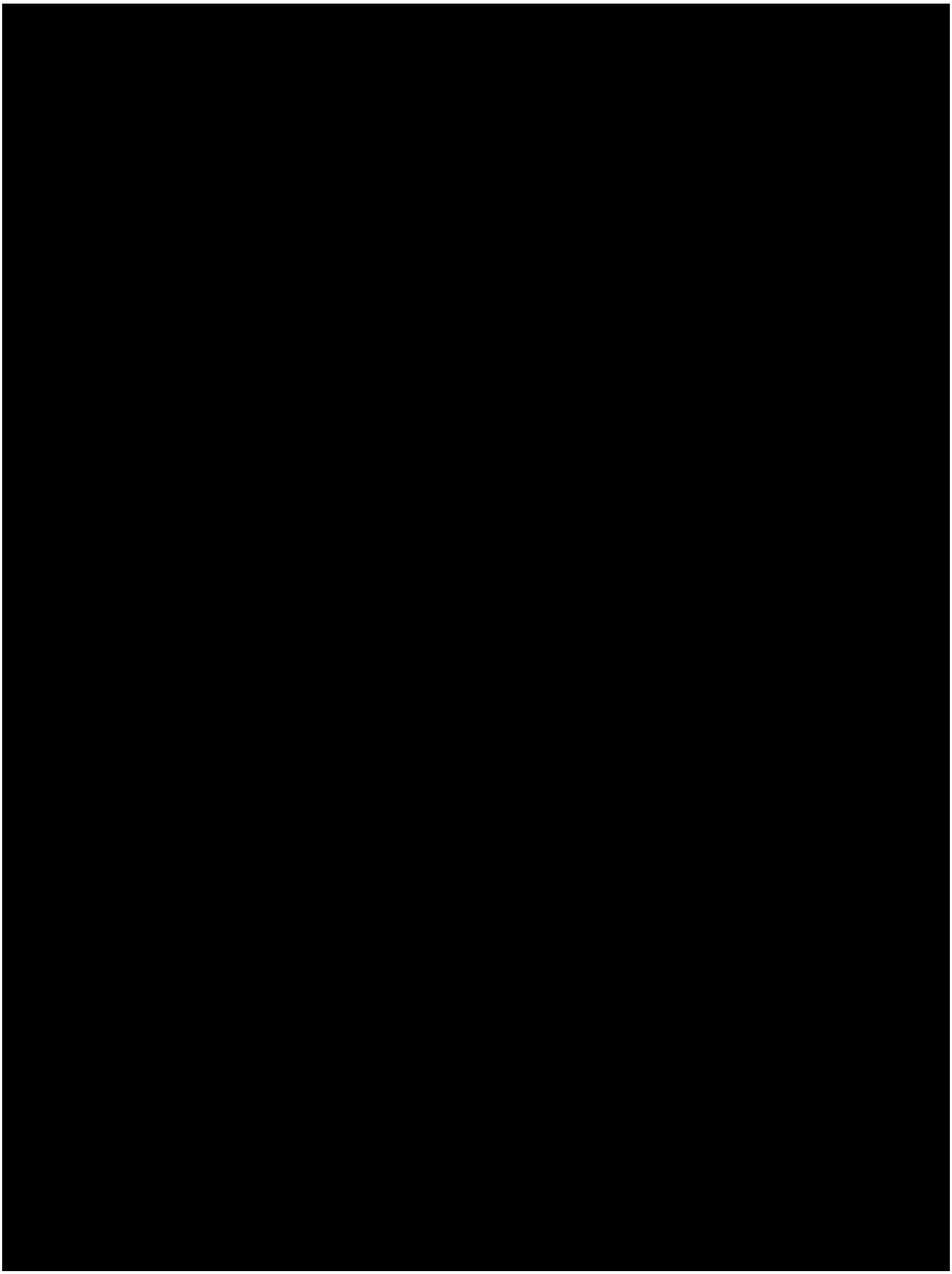
77. In addition to the above identified matters, I did a search and identified [redacted] examples of communications, work product, and other documents, which illustrate the nature of Fish's relationship with MPS, the information Fish had access to, the subject matters Fish consulted MPS on, and Fish's conflict in this matter and others since 2012. To be clear, while I identified [redacted] specific examples, they are only a small group of samples when compared to the many more communications between Fish and MPS which are relevant to the subject matter of this litigation.

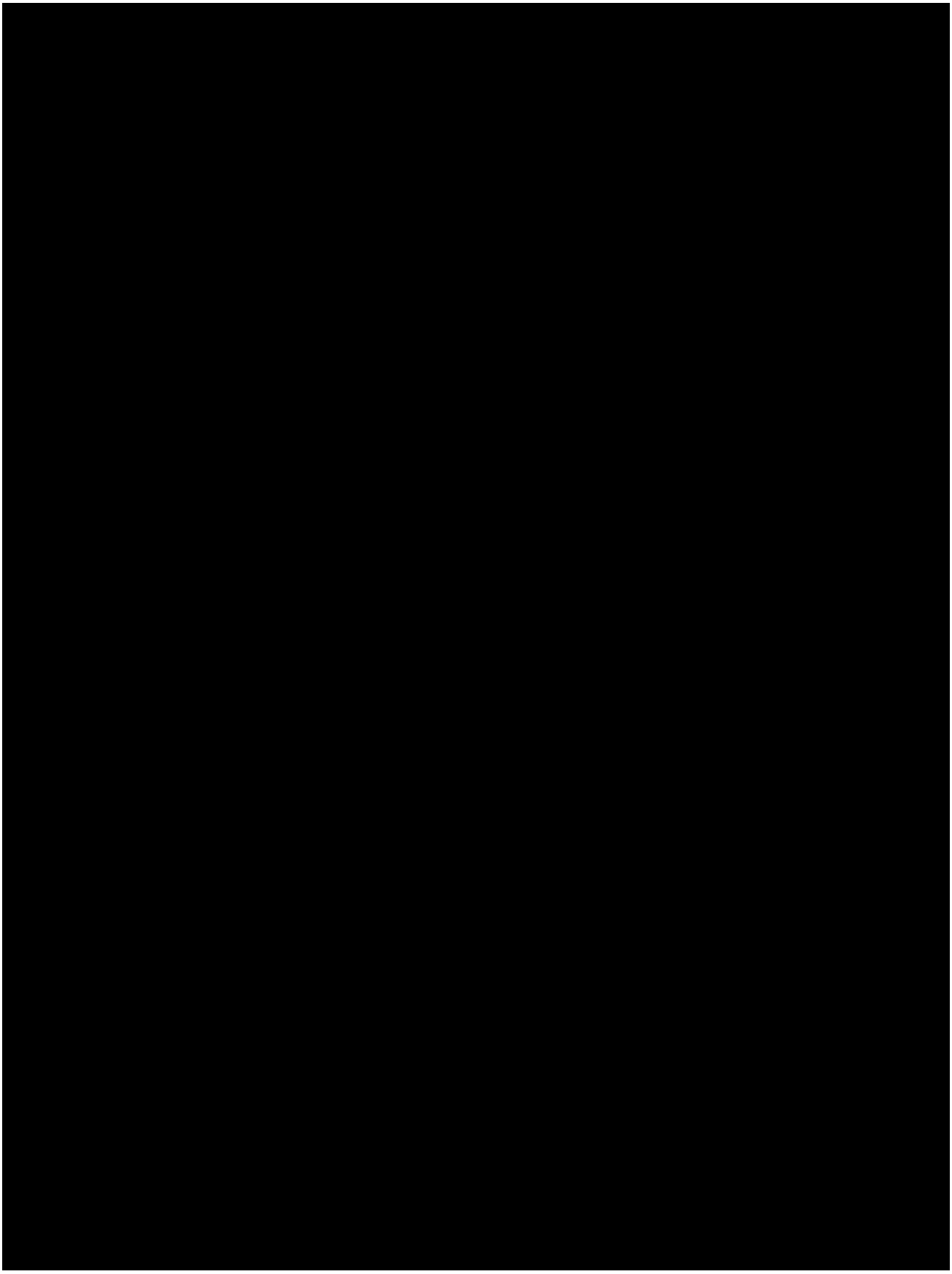
78. Due to the highly sensitive nature of these communications and documents, I have not included them as exhibits to my declaration. However, I include a list of both the documents I reference above and these further documents I located below. I note that many of the emails I reference below contain attachments as I have noted below, [redacted] Further, many of these emails were extensive email chains, so the dates, sender, and recipient fields are for referential purposes to distinguish between chains, and do not reflect all parties in each chain. Additionally, the sender and recipients of some of these messages may not be Fish and Richardson attorneys, but there is at least one FR employee who is copied (if not a direct sender or recipient) on each of the messages identified in the table. Each of these documents is available for *in camera* inspection. If needed, I can identify further communications and documents for *in camera* inspection.

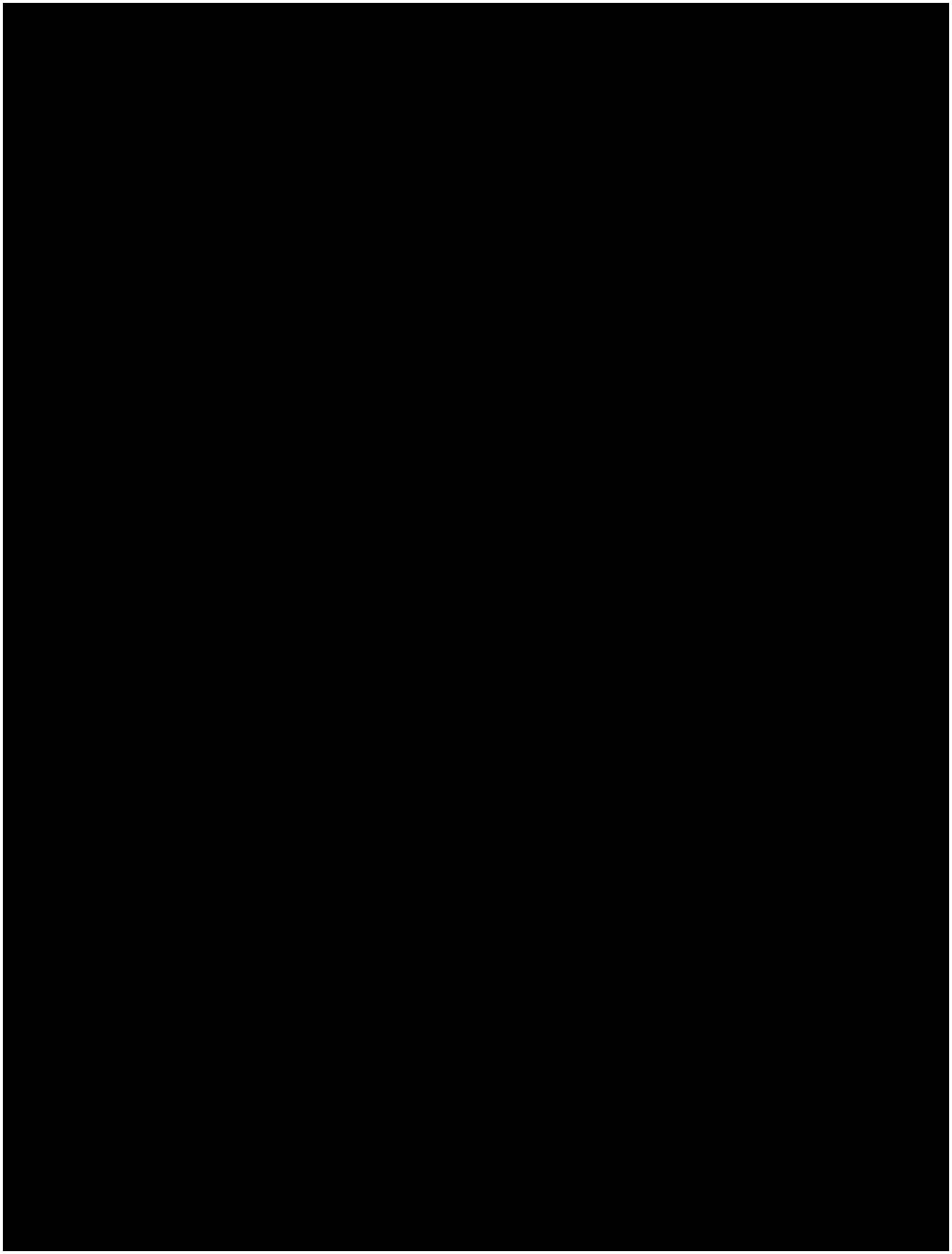
[redacted]

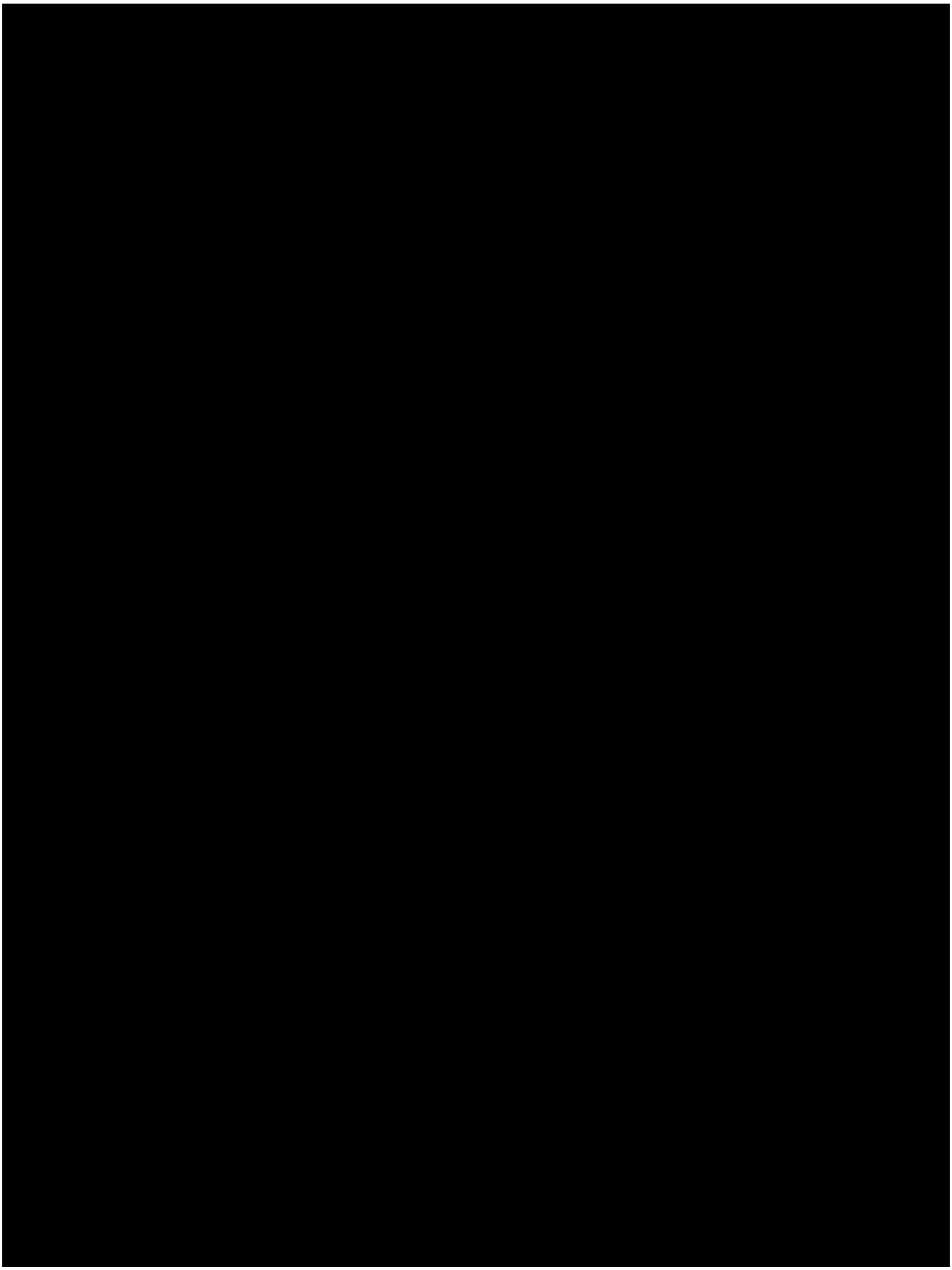


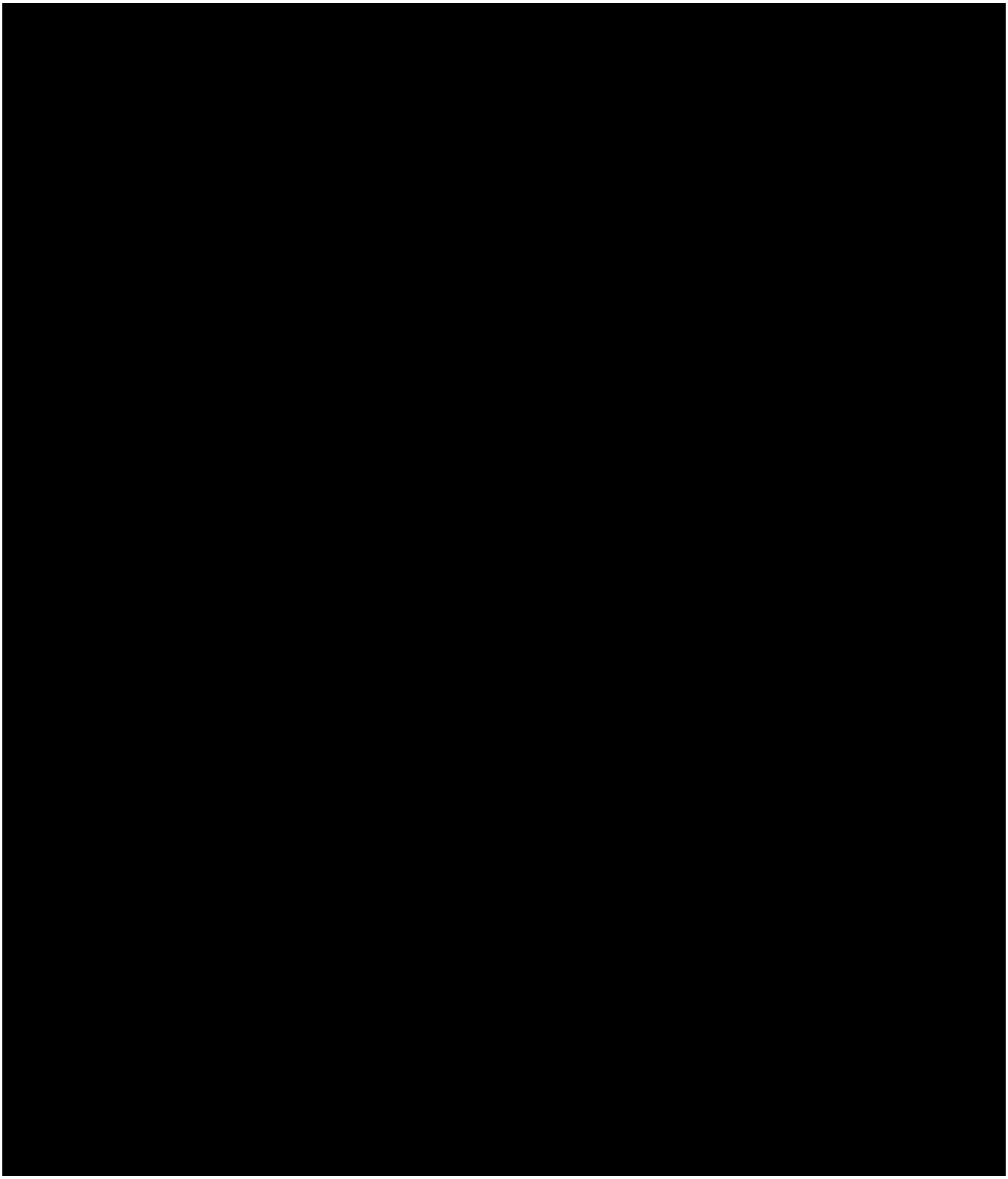






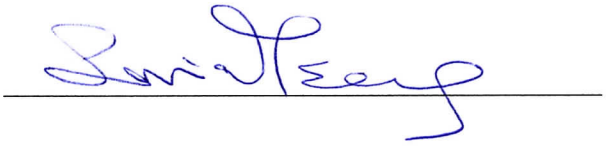






79. The foregoing is true and correct to the best of my knowledge.

Executed on April 30, 2020



CERTIFICATE OF SERVICE

I, Karen E. Keller, hereby certify that on April 30, 2020, this document was served on the persons listed below in the manner indicated:

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Exhibit 2
to
Exhibit 6

Redacted In Their Entirety

Exhibit 7

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LOS ANGELES
BY _____

UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA By Fax

CENTRAL DIVISION

Monolithic Power Systems, Inc.,

Plaintiff,

v.

Silergy Corporation

Defendant.

Case No. CV10 1533 CAS (AGRx)

COMPLAINT FOR PATENT INFRINGEMENT

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power Systems, Inc. ("MPS") hereby pleads the following claim against Defendant Silergy Corporation ("Silergy") and alleges as follows.

PARTIES

1. Plaintiff MPS is a California corporation having a principal place of business at 6409 Guadalupe Mines Road, San Jose, California 95120.

2. Defendant Silergy is, upon information and belief, a corporation organized and existing under the laws of the Cayman Islands with a principal place of business at 7F.-1, No. 202, Sec. 3, Beixin Road, Xindian City, Taipei County 231. Silergy Corporation also has a United States headquarters at 1879 Lundy Avenue, #126, San Jose, California 95131, and was a registered entity with the State of California (Entity No. C3181618) at least as of December 5, 2008. Silergy has since surrendered its status; however, Silergy continues to publicly identify its United States headquarters as the same address it previously listed for its agent for service of process. Upon information and belief, Silergy has operated and continues to operate from its United States headquarters, and is doing business throughout this judicial district and around the world.

JURISDICTION AND VENUE

3. This Court has subject matter jurisdiction over the action under 28 U.S.C. §§ 1331 and 1338(a) because the action concerns a federal question arising under the patent laws of the United States, including 35 U.S.C. § 271.

4. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(d) and 1400(b) because, among other reasons, Defendant is subject to personal jurisdiction in this judicial district, has committed acts of infringement in this judicial district, and is an alien subject to suit in this judicial district.

5. Upon information and belief, Defendant has placed infringing products into the stream of commerce by shipping those products into this judicial district (and other judicial districts) or knowing that such products would be shipped into this judicial district (and other judicial districts).

CLAIM FOR PATENT INFRINGEMENT

6. MPS incorporates by reference the allegations of paragraphs 1–6 above as fully set forth herein.

7. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 6,897,643 ("the '643 patent") entitled "Integrated Circuit Driver Having Stable Bootstrap Power Supply," which was duly and legally issued by the United States Patent and Trademark Office on May 24, 2005. A copy of the '643 patent is attached hereto as Exhibit A.

8. Silergy has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '643 patent by making, using, offering to sell, or selling in the United States, including this judicial district, or importing into the United States, step-down DC to DC converters including, but not limited to, the Silergy SY8101, SY8132, and SY8133 product families.

9. Upon information and belief, Defendant has had actual knowledge of the '643 patent.

10. Upon information and belief, infringement by Defendant of the '643 patent has been willful.

11. Past and continued acts of infringement by Defendant has injured and damaged MPS.

12. Acts of infringement by Defendant has caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MPS prays that this Court enter judgment as follows:

1. That Defendant has infringed the '643 patent;

2. That Defendant's infringement of the '643 patent is willful;

3. That Defendant, and its respective agents, servants, officers, directors, employees, and all persons acting in concert with them directly or indirectly, be enjoined from infringing the '643 patent;

4. That Defendant be ordered to account for and pay to MPS the damages arising out of its infringing activities, together with interest and costs, and all other damages permitted by 35 U.S.C. § 284, including enhanced damages up to three times the amount of damages found or measured;

5. That this action be adjudged an exceptional case and that MPS be awarded its attorneys' fees, expenses and costs in this action pursuant to 35 U.S.C. § 285; and

6. That MPS be awarded such other equitable or legal relief as this Court deems just and proper under the circumstances.

DEMAND FOR JURY TRIAL

MPS demands a trial by jury on all issues so triable.

Dated: March 1, 2010

FISH & RICHARDSON P.C.

By: _____
John P. Schnurer

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power Systems, Inc. demands a jury trial on all claims and issues.

Dated: March 1, 2010

FISH & RICHARDSON P.C.

By: _____
John P. Schnurer

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

EXHIBIT A

US006897643B2

(12) **United States Patent**
Stone

(10) **Patent No.: US 6,897,643 B2**
(45) **Date of Patent: May 24, 2005**

(54) **INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY**

(75) Inventor: **Marshall David Stone**, Fremont, CA (US)

(73) Assignee: **Monolithic Power Systems, Inc.**, Los Gatos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.

(21) Appl. No.: **10/269,617**

(22) Filed: **Oct. 11, 2002**

(65) **Prior Publication Data**

US 2004/0070383 A1 Apr. 15, 2004

(51) **Int. Cl.**[7] **G05F 1/40**; H03K 17/60

(52) **U.S. Cl.** **323/288**; 323/224; 327/390; 327/589

(58) **Field of Search** 323/288, 224, 323/286, 282, 289, 225, 284, 285, 287; 363/60, 98, 17, 56, 132; 327/387, 390, 374–377, 434, 589, 537, 538, 536; 307/910, 475, 482, 578

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,883,978	A *	11/1989	Ohshima et al.	326/24
5,365,118	A	11/1994	Wilcox	
5,550,436	A	8/1996	Houk	
5,627,460	A *	5/1997	Bazinet et al.	323/288
5,828,262	A *	10/1998	Rees	327/390
6,172,493	B1 *	1/2001	Grant	323/288
6,462,522	B2 *	10/2002	Burstein et al.	323/282
6,661,208	B2 *	12/2003	Rutter et al.	323/224
2002/0036487	A1	3/2002	Moriconi et al.	

* cited by examiner

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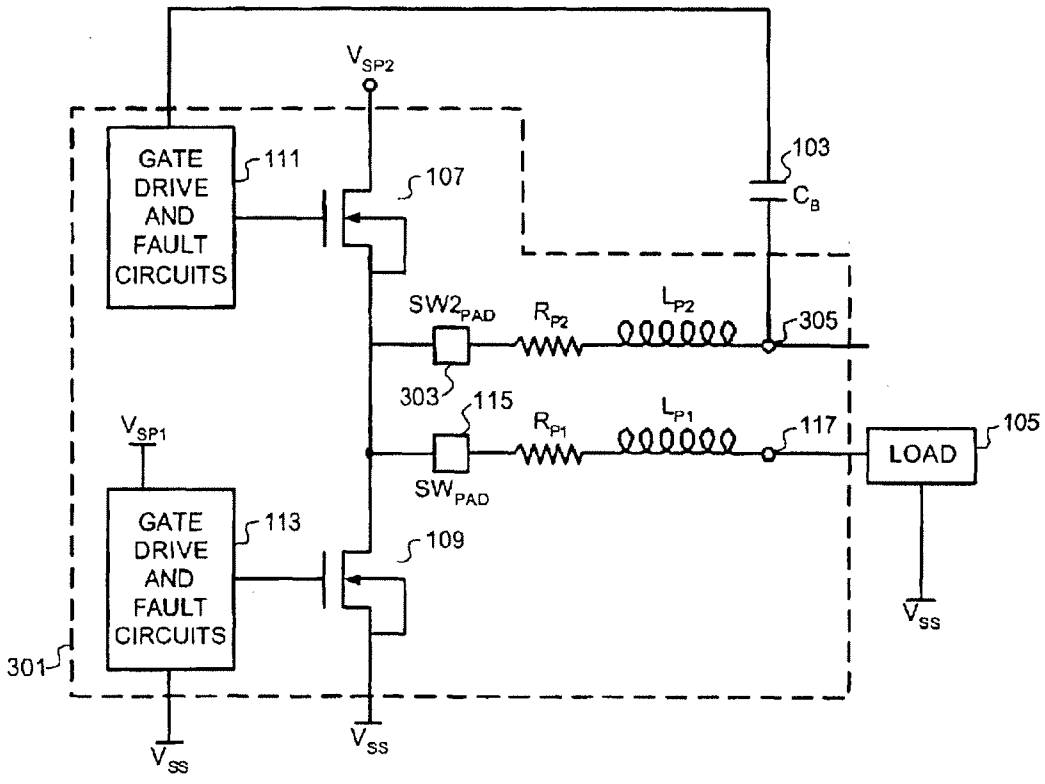
(57) **ABSTRACT**

An integrated circuit driver is disclosed. The driver comprises a high side transistor and a low side transistor connected in series. The output of the driver is taken from the source of the high side transistor and the drain of the low side transistor. A bootstrap contact pad is connected to the output node. Connected to the bootstrap contact pad is a bootstrap capacitor that is also connected to a high side gate drive that selectively controls the high side transistor.

14 Claims, 4 Drawing Sheets



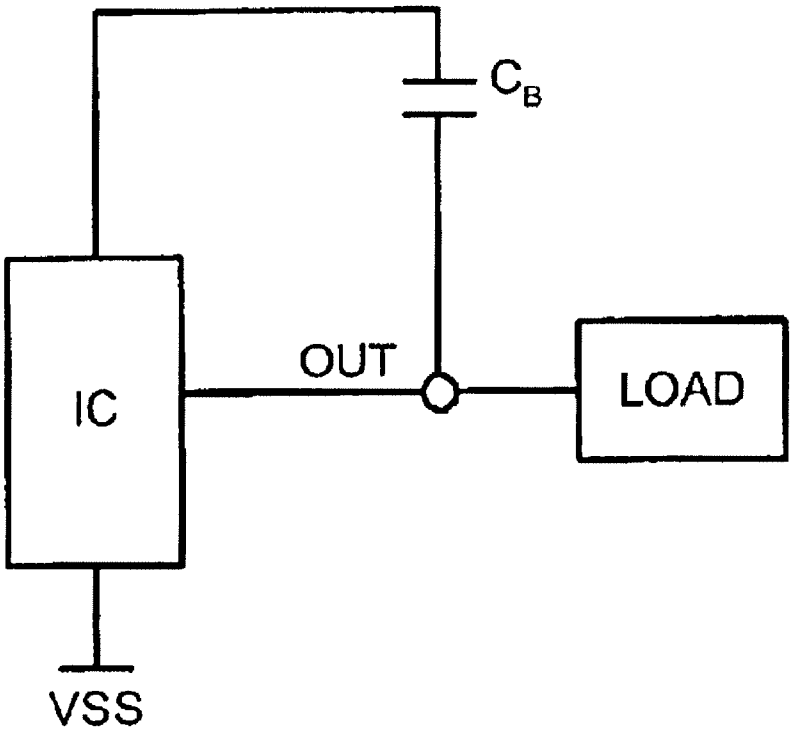


FIGURE 1
(PRIOR ART)

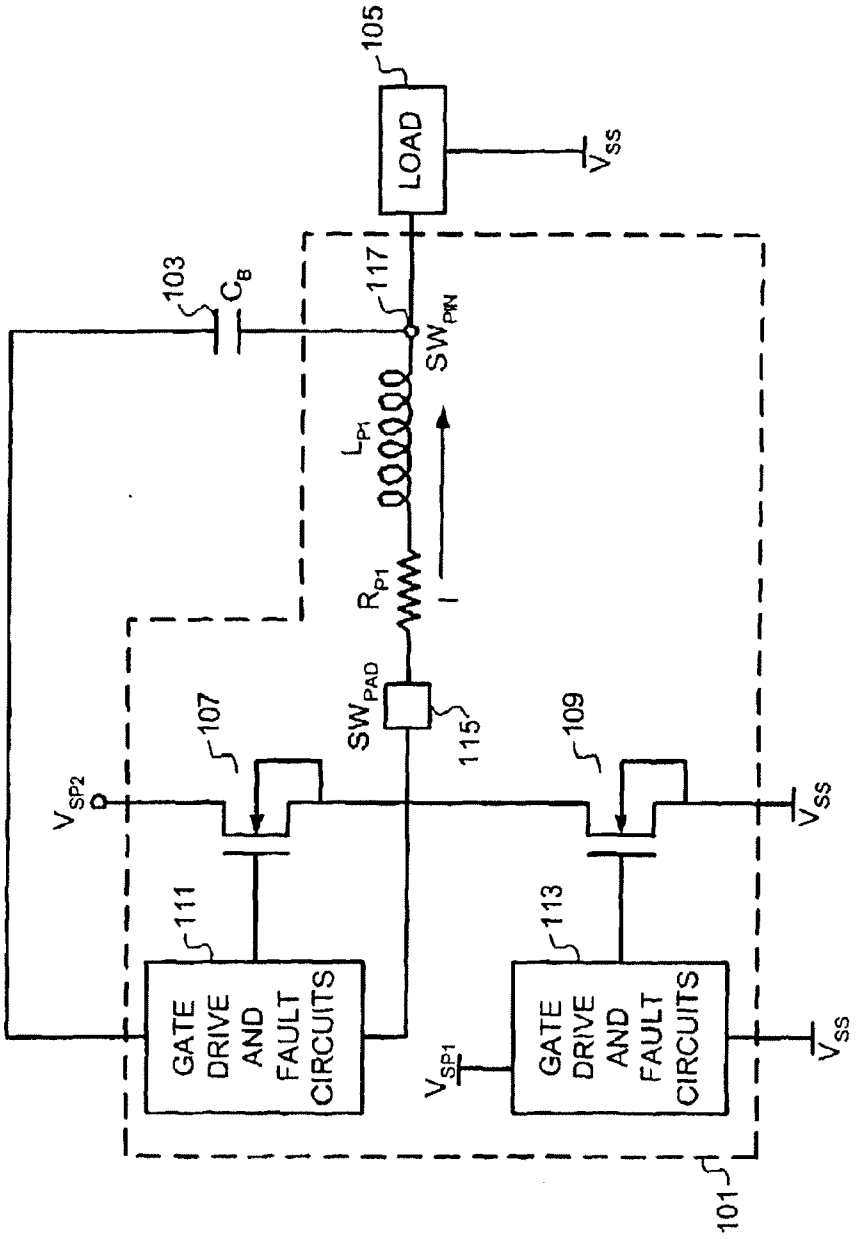


FIGURE 2
(PRIOR ART)

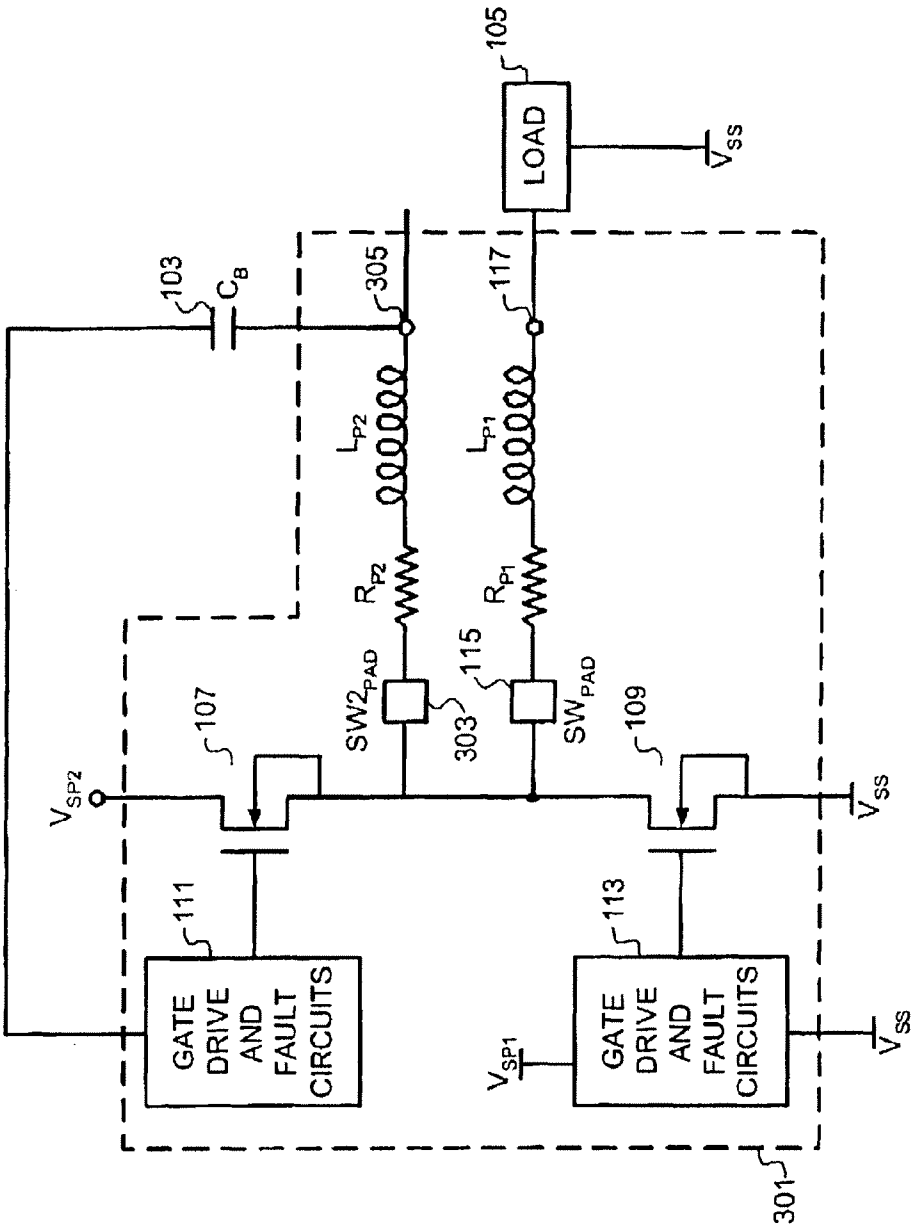

105
LOAD
V_{SS}
103
C_B
305
117
L_{P2}
L_{P1}
R_{P2}
R_{P1}
$SW2_{PAD}$
115
303
SW_{PAD}
107
109
V_{SP2}
V_{SS}
111
113
GATE DRIVE AND FAULT CIRCUITS
V_{SP1}
GATE DRIVE AND FAULT CIRCUITS
V_{SS}
301

FIGURE 3

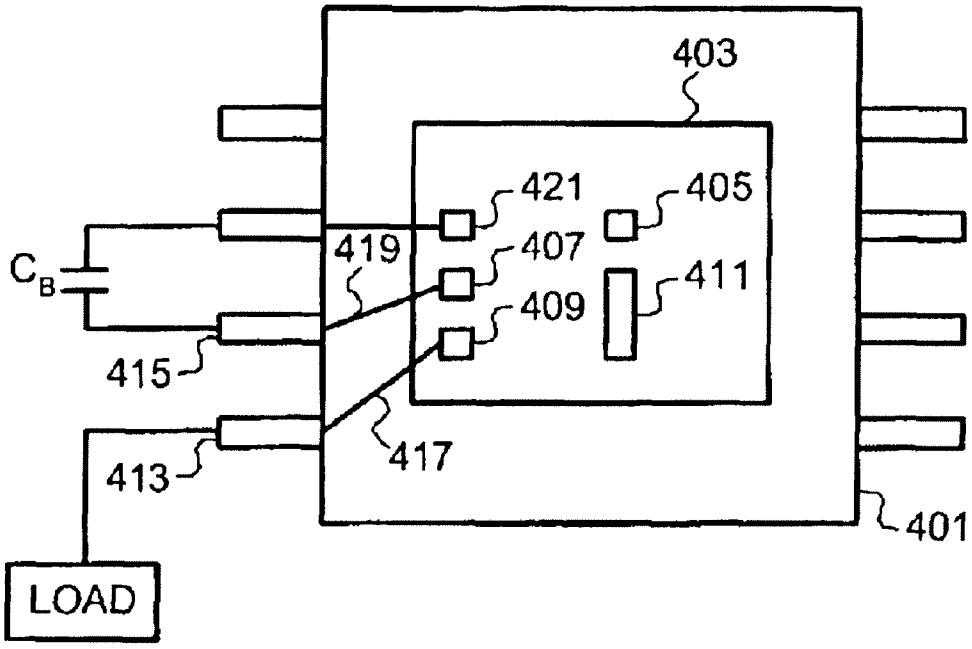


FIGURE 4

INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY

TECHNICAL FIELD

The present invention relates to integrated circuit drivers that use a bootstrap supply to drive the gate of the high side switch, and more particularly, to a method and apparatus for providing a stable bootstrap voltage to the gate of the high side switch.

BACKGROUND

One common type of integrated circuit driver utilizes two power MOSFET switches in a totem pole (half-bridge) topology. The MOSFET switches are typically NMOS switches that are connected in series. The power MOSFET switches are driven to conduct alternately. One of the MOSFET switches is designated as a high side switch, and the other MOSFET switch is designated as the low side switch. In one application, by selectively switching the power MOSFET switches in an alternating fashion, a load can be driven with an alternating current. In such a manner, a DC to AC inverter is formed. Likewise by controlling the switches according to an input signal (such as an acoustic signal), a class D audio amplifier is formed. Further, the same half bridge topology using a stable DC reference as the input can be used to create a DC power supply.

The gate of the high side switch is typically driven by a bootstrapped power supply. This is done to allow use of an NMOS switch, which has roughly half the on resistance of a PMOS switch of the same area. A bootstrap capacitor is used to increase the voltage available to the gate of the high side switch. FIG. **1** shows a prior art simplified schematic of an integrated circuit driver (IC) used in conjunction with a bootstrap capacitor to drive a load. The IC driver provides current to drive a load. A bootstrap capacitor C_b has one terminal connected to the output of the IC driver. The other terminal of the bootstrap capacitor C_b is provided back to the IC driver to drive the gate of the high side switch.

A more detailed schematic of the IC driver of FIG. **1** is shown in FIG. **2**. As seen in FIG. **2**, the IC driver **101** includes the high side switch **107** and the low side switch **109**. The high side switch **107** is driven by gate drive and fault circuit **111**. Similarly, the low side switch **109** is driven by gate drive and fault circuit **113**. The gate drive and fault circuits **111** and **113** are operative to control the switching of the high side and low side switches **107** and **109**. In addition, the gate drive and fault circuits **111** and **113** typically include fault detection circuitry and a bootstrap supply monitor. These additional functions are generally needed to measure whether there is a fault condition on the switch or whether the bootstrap supply is sufficient for the IC to operate properly.

The precise configuration of the gate drive and fault circuits **111** and **113** may be varied, but generally the configuration and operation is well known in the prior art. Note that the gate drive and fault circuit **113** used to control the low side switch **109** operates using a first supply voltage V_{sp1}. The low side switch **109** does not require a bootstrapped power supply. In contrast, the gate drive and fault circuit **111** that controls the high side switch **107** is connected to the bootstrap capacitor **103**.

The output of the IC driver **101** is taken from the node connecting the high side switch and the low side switch. In physical terms, the output node is a conductive pad on the integrated circuit, designated in FIG. **2** as SW_{pad} **115**. The integrated circuit die is then set into a package wherein the pad SW_{pad} **115** is connected to a package pin SW_{pin} **117**. The connection between the pad **115** and the package pin **117** is typically made through a bond wire formed of gold, copper, or other highly conductive material.

Nevertheless, the bond wire between the pad **115** and the package pin **117** includes some finite amount of parasitic inductance L_{p1} and parasitic resistance R_{p1}. When current is supplied through the pin **117** to the load **105**, invariably there will be a loss of voltage across the parasitic inductance L_{p1} and parasitic resistance R_{p1}.

The amount of the voltage drop is important because any voltage that develops across the bond wire between SW pad and SW pin, subtracts directly and instantaneously from the bootstrap supply. Because of the large value of current and high rate of change of that current in the bondwire, the voltage drop can be significant, on the order of two or more volts. This sudden drop in the internal bootstrap supply voltage will adversely affect any signal processing operating under the internal bootstrap supply, such as the bootstrap supply monitor and fault check circuits.

Therefore, the arrangement shown in FIG. **2** having an imprecise and noisy bootstrap supply is undesirable.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram showing a bootstrap capacitor and an integrated circuit driver for driving a load.

FIG. **2** is a detailed schematic of the integrated circuit driver of FIG. **1**.

FIG. **3** is a schematic circuit diagram illustrating one embodiment of the present invention.

FIG. **4** is an illustration of an integrated circuit die mounted on an integrated circuit package.

DETAILED DESCRIPTION

The present invention is an integrated circuit driver having a "quieter" bootstrap power supply. The integrated circuit driver has an output pin and output pad that is dedicated to the bootstrap capacitor thereby maintaining a stable bootstrap supply voltage. In the following description, some specific details, such as example values for the circuit components, are provided to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

FIG. **3** shows one embodiment of the present invention. As seen, FIG. **3** is substantially similar to the prior art IC driver **101**, except that an additional pad $SW2_{pad}$ **303** is also attached to the output node between the high side switch **107** and the low side switch **109**. Additionally, a second output pin **305** is provided from the IC driver **301**. Having the second pad **303** and the second package pin **305** connected to the bootstrap capacitor **103**, the bootstrap capacitor **103** is not affected by any voltage drop caused by current flowing to the load **105** through a first package pin **117**.

Note that substantially all the current provided by the high side switch **107** and the low side switch **109** flows to the load **105** through the package pin **117**. Little if any current flows through the second package pin **305**, thereby eliminating any voltage drop through the parasitic resistance and inductance of the bond wire connecting the second package pin **305** to the second pad **303**. Thus, the bootstrap supply voltage provided by the bootstrap capacitor **103** maintains its value and is less noisy.

As seen, the IC driver **301** of the present invention includes an additional package pin **305** that is connected directly to the bootstrap capacitor **103**. In an alternative embodiment, the second package pin **305** has a bond wire directly attached to the same pad **115** as the first package pin **117**. This saves the requirement for forming the second pad **303**. In one embodiment, the IC driver **301** may be used to drive, for example, a cold-cathode fluorescent lamp. However, typically, the lamp is connected through a secondary winding of a transformer whose primary winding is connected to the output of the IC driver **301**.

FIG. **4** further illustrates the arrangement of the present invention. In FIG. **4**, an integrated circuit package **401** is adapted to mount an integrated circuit die **403**. The integrated circuit die **403** includes various circuitry, such as the low side switch, the high side switch, and the gate drive and fault circuitry. In addition, the integrated circuit die **403** includes an output contact pad **409**, a bootstrap contact pad **407** (referred to as a second pad $SW2_{pad}$ **303** in FIG. **3**), a high side gate drive input pad **421**, and various other contact pads **405** and **411**.

The output contact pad **409** is connected to an output pin **413** of the integrated circuit package **401** by an output bond wire **417**. The output bond wire **417** is secured to the output pin **413** and the output contact pad **409**. The bootstrap contact pad **407** is connected to bootstrap pin **415** of the integrated circuit package **401** by a bootstrap bond wire **419**. The bootstrap bond wire **419** is secured to the bootstrap pin **415** and the bootstrap contact pad **407**.

The bootstrap capacitor C_b is connected between the bootstrap pin **415** and the gate drive circuitry on the integrated circuit **403** through another package pin and high side gate drive input pad **421**. Finally, the load is connected to the output pin **413**. The other various pins of the integrated circuit package **401** are used in known configurations, such as for power supply, ground, control lines, and such.

As noted above, in an alternate embodiment, the output contact pad **409** and the bootstrap contact pad **407** is one and the same. Whichever pad conducts current to the load is made large, such as contact pad **411**, but not changed in size if also attached to Cb.

Thus, the above described IC driver provides a stable bootstrap power supply, even when large amounts of power are being delivered. This is accomplished by connecting the bootstrap capacitor to a dedicated bootstrap pin and contact pad.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein

for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a bootstrap contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap contact pad, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output contact pad connected to the output node, said output contact pad providing an output signal to a load.

2. The driver of claim **1** wherein said high side transistor and said low side transistor are NMOS transistors.

3. The driver of claim **1** wherein said output contact pad and said bootstrap contact pad are the same.

4. The driver of claim **1** further including an output package pin connected to said output pad by an output bond wire.

5. The driver of claim **1** further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

6. The driver of claim **3** further including an output package pin connected to said output pad by an output bond wire.

7. The driver of claim **3** further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

8. An integrated circuit package comprising:

(a) an integrated circuit die, said die having formed thereon:

(1) a high side transistor;

(2) a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

(3) a set of two bootstrap contact pads connected to the output node;

(4) a high side gate drive for selectively controlling the high side transistor;

(5) a low side gate drive for selectively controlling the low side transistor; and

(6) a set of two output contact pads connected to the output node, said output contact pads providing output signals to a load;

(b) a set of two carrier packages having a plurality of package pins including at least a bootstrap package pin and an output package pin, said carrier packages for securing said integrated circuit die;

(c) a set of two output bond wires connecting said output contact pads with said output package pins; and

(d) a set of two bootstrap bond wires connecting said bootstrap contact pads with said bootstrap package pins.

9. The package of claim **8** wherein said high side transistor and said low side transistor are NMOS transistors.

10. The package of claim **8** wherein said output contact pad and said bootstrap contact pad are the same.

11. The package of claim **8** wherein a first terminal of a bootstrap capacitor is connected to said bootstrap package pin and a second terminal of said bootstrap capacitor is connected to an input to said high side gate drive.

12. A method for driving a load using a high side switch and a low side switch connected in series, the source of said high side switch connected to the drain of said low side switch, the connection of said high side switch and said low side switch being an output node, the method comprising:

providing a bootstrap contact pad connected to said output node;

providing an output pad connected to said output node;

connecting a bootstrap capacitor to said bootstrap contact pad, said bootstrap capacitor used to provide a bootstrap power supply to a gate drive of said high side switch, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor; and

connecting said output pad to said load.

13. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a combination bootstrap/output contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap/output contact pad via a bootstrap capacitor package pin, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output package pin connecting said bootstrap/output contact pad to a load.

14. The driver of claim **13** wherein said high side transistor and said low side transistor are NMOS transistors.

* * * * *

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UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA

CIVIL COVER SHEET

I (a) PLAINTIFFS (Check box if you are representing yourself ☐)	DEFENDANTS
Monolithic Power Systems, Inc.	Silergy Corporation
(b) Attorneys (Firm Name, Address and Telephone Number. If you are representing yourself, provide same.) John P. Schnurer Fish & Richardson P.C. 555 West Fifth Street, 31st Floor Los Angeles, CA 90013 213-533-4240 schnurer@fr.com	Attorneys (If Known)

By Fax

II. BASIS OF JURISDICTION (Place an X in one box only.)

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question (U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity (Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES - For Diversity Cases Only (Place an X in one box for plaintiff and one for defendant.)

	PTF	DEF		PTF	DEF
Citizen of This State	☐ 1	☐ 1	Incorporated or Principal Place of Business in this State	☐ 4	☐ 4
Citizen of Another State	☐ 2	☐ 2	Incorporated and Principal Place of Business in Another State	☐ 5	☐ 5
Citizen or Subject of a Foreign Country	☐ 3	☐ 3	Foreign Nation	☐ 6	☐ 6

IV. ORIGIN (Place an X in one box only.)

☒ 1 Original Proceeding ☐ 2 Removed from State Court ☐ 3 Remanded from Appellate Court ☐ 4 Reinstated or Reopened ☐ 5 Transferred from another district (specify): ☐ 6 Multi-District Litigation ☐ 7 Appeal to District Judge from Magistrate Judge

V. REQUESTED IN COMPLAINT: JURY DEMAND: ☒ Yes ☐ No (Check 'Yes' only if demanded in complaint.)

CLASS ACTION under F.R.C.P. 23: ☐ Yes ☒ No ☒ MONEY DEMANDED IN COMPLAINT: $ any unspecified

VI. CAUSE OF ACTION (Cite the U.S. Civil Statute under which you are filing and write a brief statement of cause. Do not cite jurisdictional statutes unless diversity.)

VII. NATURE OF SUIT (Place an X in one box only.)

OTHER STATUTES	CONTRACT	REAL PROPERTY	TORTS	PRISONER PETITIONS	LABOR
☐ 400 State Reapportionment	☐ 110 Insurance	PERSONAL INJURY	PERSONAL PROPERTY	☐ 510 Motions to Vacate Sentence Habeas Corpus	☐ 710 Fair Labor Standards Act
☐ 410 Antitrust	☐ 120 Marine	☐ 310 Airplane	☐ 370 Other Fraud	☐ 530 General	☐ 720 Labor/Mgmt. Relations
☐ 430 Banks and Banking	☐ 130 Miller Act	☐ 315 Airplane Product Liability	☐ 371 Truth in Lending	☐ 535 Death Penalty	☐ 730 Labor/Mgmt. Reporting & Disclosure Act
☐ 450 Commerce/ICC Rates/etc.	☐ 140 Negotiable Instrument	☐ 320 Assault, Libel & Slander	☐ 380 Other Personal Property Damage	☐ 540 Mandamus/ Other	☐ 740 Railway Labor Act
☐ 460 Deportation	☐ 150 Recovery of Overpayment & Enforcement of Judgment	☐ 330 Fed. Employers' Liability	☐ 385 Property Damage Product Liability	☐ 550 Civil Rights	☐ 790 Other Labor Litigation
☐ 470 Racketeer Influenced and Corrupt Organizations	☐ 151 Medicare Act	☐ 340 Marine	BANKRUPTCY	☐ 555 Prison Condition	☐ 791 Empl. Ret. Inc. Security Act
☐ 480 Consumer Credit	☐ 152 Recovery of Defaulted Student Loan (Excl. Veterans)	☐ 345 Marine Product Liability	☐ 422 Appeal 28 USC 158	FORFEITURE/PENALTY	PROPERTY RIGHTS
☐ 490 Cable/Sat TV	☐ 153 Recovery of Overpayment of Veteran's Benefits	☐ 350 Motor Vehicle	☐ 423 Withdrawal 28 USC 157	☐ 610 Agriculture	☐ 820 Copyrights
☐ 810 Selective Service	☐ 160 Stockholders' Suits	☐ 355 Motor Vehicle Product Liability	CIVIL RIGHTS	☐ 620 Other Food & Drug	☒ 830 Patent
☐ 850 Securities/Commodities/ Exchange	☐ 190 Other Contract	☐ 360 Other Personal Injury	☐ 441 Voting	☐ 625 Drug Related Seizure of Property 21 USC 881	☐ 840 Trademark
☐ 875 Customer Challenge 12 USC 3410	☐ 195 Contract Product Liability	☐ 362 Personal Injury-Med Malpractice	☐ 442 Employment	☐ 630 Liquor Laws	SOCIAL SECURITY
☐ 890 Other Statutory Actions	☐ 196 Franchise	☐ 365 Personal Injury-Product Liability	☐ 443 Housing/Accommodations	☐ 640 R.R. & Truck	☐ 861 HIA (1395ff)
☐ 891 Agricultural Act	REAL PROPERTY	☐ 368 Asbestos Personal Injury Product Liability	☐ 444 Welfare	☐ 650 Airline Regs	☐ 862 Black Lung (923)
☐ 892 Economic Stabilization Act	☐ 210 Land Condemnation	IMMIGRATION	☐ 445 American with Disabilities - Employment	☐ 660 Occupational Safety/Health	☐ 863 DIWC/DIWW (405(g))
☐ 893 Environmental Matters	☐ 220 Foreclosure	☐ 462 Naturalization Application	☐ 446 American with Disabilities - Other	☐ 690 Other	☐ 864 SSID Title XVI
☐ 894 Energy Allocation Act	☐ 230 Rent Lease & Ejectment	☐ 463 Habeas Corpus-Alien Detainee	☐ 440 Other Civil Rights		☐ 865 RSI (405(g))
☐ 895 Freedom of Info. Act	☐ 240 Torts to Land	☐ 465 Other Immigration Actions			FEDERAL TAX SUITS
☐ 900 Appeal of Fee Determination Under Equal Access to Justice	☐ 245 Tort Product Liability				☐ 870 Taxes (U.S. Plaintiff or Defendant)
☐ 950 Constitutionality of State Statutes	☐ 290 All Other Real Property				☐ 871 IRS - Third Party 26 USC 7609

FOR OFFICE USE ONLY: Case Number: CV10 1533

AFTER COMPLETING THE FRONT SIDE OF FORM CV-71, COMPLETE THE INFORMATION REQUESTED BELOW.

UNITED STATES DISTRICT COURT, CENTRAL DISTRICT OF CALIFORNIA
CIVIL COVER SHEET

VIII(a). IDENTICAL CASES: Has this action been previously filed in this court and dismissed, remanded or closed? [X] No [ ] Yes

If yes, list case number(s):

VIII(b). RELATED CASES: Have any cases been previously filed in this court that are related to the present case? [X] No [ ] Yes

If yes, list case number(s):

Civil cases are deemed related if a previously filed case and the present case:

(Check all boxes that apply)

- [ ] A. Arise from the same or closely related transactions, happenings, or events; or
- [ ] B. Call for determination of the same or substantially related or similar questions of law and fact; or
- [ ] C. For other reasons would entail substantial duplication of labor if heard by different judges; or
- [ ] D. Involve the same patent, trademark or copyright, and one of the factors identified above in a, b or c also is present.

IX. VENUE: (When completing the following information, use an additional sheet if necessary.)

(a) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named plaintiff resides.

[ ] Check here if the government, its agencies or employees is a named plaintiff. If this box is checked, go to item (b).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Santa Clara County	

(b) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** named defendant resides.

[ ] Check here if the government, its agencies or employees is a named defendant. If this box is checked, go to item (c).

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
N/A Defendant is a Taiwanese company.	

(c) List the County in this District; California County outside of this District; State if other than California; or Foreign Country, in which **EACH** claim arose.

Note: In land condemnation cases, use the location of the tract of land involved.

County in this District:*	California County outside of this District; State, if other than California; or Foreign Country
Los Angeles County	

*** Los Angeles, Orange, San Bernardino, Riverside, Ventura, Santa Barbara, or San Luis Obispo Counties**

Note: In land condemnation cases, use the location of the tract of land involved

X. SIGNATURE OF ATTORNEY (OR PRO PER): _____ **Date** March 1, 2010

John P. Schnurer

Notice to Counsel/Parties: The CV-71 (JS-44) Civil Cover Sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law. This form, approved by the Judicial Conference of the United States in September 1974, is required pursuant to Local Rule 3-1 is not filed but is used by the Clerk of the Court for the purpose of statistics, venue and initiating the civil docket sheet. (For more detailed instructions, see separate instructions sheet.)

Key to Statistical codes relating to Social Security Cases:

Nature of Suit Code	Abbreviation	Substantive Statement of Cause of Action
861	HIA	All claims for health insurance benefits (Medicare) under Title 18, Part A, of the Social Security Act, as amended. Also, include claims by hospitals, skilled nursing facilities, etc., for certification as providers of services under the program. (42 U.S.C. 1935FF(b))
862	BL	All claims for "Black Lung" benefits under Title 4, Part B, of the Federal Coal Mine Health and Safety Act of 1969. (30 U.S.C. 923)
863	DIWC	All claims filed by insured workers for disability insurance benefits under Title 2 of the Social Security Act, as amended; plus all claims filed for child's insurance benefits based on disability. (42 U.S.C. 405(g))
863	DIWW	All claims filed for widows or widowers insurance benefits based on disability under Title 2 of the Social Security Act, as amended. (42 U.S.C. 405(g))
864	SSID	All claims for supplemental security income payments based upon disability filed under Title 16 of the Social Security Act, as amended.
865	RSI	All claims for retirement (old age) and survivors benefits under Title 2 of the Social Security Act, as amended. (42 U.S.C. (g))

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AO 440 (Rev. 02/09) Summons in a Civil Action

UNITED STATES DISTRICT COURT

for the

CENTRAL DISTRICT OF CALIFORNIA

Monolithic Power Systems, Inc.

Plaintiff

v.

Silergy Corporation

Defendant

CV10 1533 CAS (AGRx)

Civil Action No.

By Fax

SUMMONS IN A CIVIL ACTION

To: *(Defendant's name and address)*

SILERGY CORPORATION

A lawsuit has been filed against you.

Within 21 days after service of this summons on you (not counting the day you received it) — or 60 days if you are the United States or a United States agency, or an officer or employee of the United States described in Fed. R. Civ. P. 12 (a)(2) or (3) — you must serve on the plaintiff an answer to the attached complaint or a motion under Rule 12 of the Federal Rules of Civil Procedure. The answer or motion must be served on the plaintiff or plaintiff's attorney, whose name and address are:

John P. Schnurer, SBN 185725
schnurer@fr.com
FISH & RICHARDSON P.C.
555 West Fifth Street, 31st Floor
Los Angeles, CA 90013
Telephone: (213) 533-4240

If you fail to respond, judgment by default will be entered against you for the relief demanded in the complaint. You also must file your answer or motion with the court.

CLERK OF COURT

Date: MAR - 2 2010

CHRISTOPHER POWERS

Signature of Clerk or Deputy Clerk

SEAL

AO440

Exhibit 8

9/21 DIVERSIFIED LEGAL SERVICES, INC 619-260-0316 1

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Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA
WESTERN DIVISION

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MONOLITHIC POWER SYSTEMS, INC.,

Plaintiff,

v.

SILERGY CORPORATION and SILERGY TECHNOLOGY,

Defendants.

Case No. CV-10-01533 CAS (AGRx)s

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT

JURY TRIAL DEMANDED

COPY

Plaintiff Monolithic Power Systems, Inc. ("MPS) hereby pleads the following claim against Defendants Silergy Corporation ("Silergy Corp.") and Silergy Technology ("Silergy Tech") and alleges as follows.

PARTIES

1. Plaintiff MPS is a California corporation having a principal place of business at 6409 Guadalupe Mines Road, San Jose, California 95120.

2. Defendant Silergy Corp. is, upon information and belief, a corporation organized and existing under the laws of the Cayman Islands with a principal place of business at 7F.-1 No. 202, Sec. 3, Beixin Road, Xindian City, Taipei County 231. Silergy Corp. also has a United States headquarters at 1879 Lundy Avenue, #126, San Jose, California 95131, and was a registered entity with the State of California (Entity No. C3181618) at least as of December 5, 2008. Silergy Corp. has since surrendered its status; however, Silergy Corp. continues to publicly identify its United States headquarters as the same address it previously listed for its agents for service of process. Upon information and belief, Silergy Corp. has operated and continues to operate from its United States headquarters, and is doing business throughout this judicial district and around the world.

3. Defendant Silergy Tech. is, upon information and belief, a corporation organized and existing under the laws of the state of California, with a principal place of

business at 1309 S. Mary Ave., #215, Sunnyvale, CA, 94087. Silergy Tech. has appointed its agent for service as follows: Xin Shao, 2570 N. First Street, #208, San Jose, California 95131. Upon information and belief, Silergy Tech is an affiliated entity to Silergy Corp., including being under at least partially common control with Silergy Corp., and obtaining United States Patents for Silergy Corp.'s benefit.

4. Silergy Corp. and Silergy Tech. are hereinafter referred to collectively as "Silergy."

JURISDICTION AND VENUE

5. This court has subject matter jurisdiction over the action at least under 28 U.S.C. §§ 1331 and 1338(a) because the action concerns a federal question arising under the patent laws of the United States, including 35 U.S.C. § 271.

6. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(d) and 1400(b) because, among other reasons and based on information and belief, Silergy is subject to personal jurisdiction in this judicial district, has committed acts of infringement in this judicial district, and because Silergy Corp. is an alien subject to suit in this judicial district.

7. Upon information and belief, Silergy has designed, manufactured, and placed infringing products into the stream of commerce by shipping those products into this judicial district (and other judicial districts) or knowing that such products would be shipped into this judicial district (and other judicial districts) by third parties, including

at least placing the infringing Silergy products in Acer® AO533 notebook computers manufactured by third party Acer Inc. for shipping into this judicial district.

CLAIM I: INFRINGEMENT OF U.S. PATENT NO. 6,897,643

8. MPS incorporates by reference the allegations of paragraphs 1-7 above as fully set forth herein.

9. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 6,897,643 ("the '643 Patent") entitled "Integrated Circuit Driver Having Stable Bootstrap Power Supply," which was duly and legally issued by the United States Patent and Trademark Office on May 24,2005. A copy of the '643 Patent is attached hereto as Exhibit A.

10. Silergy has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '643 Patent by making, using, offering to sell, selling, and/or other acts constituting infringement under 35 U.S.C. § 271 in the United States, including this judicial district, or importing into the United States, step-down DC to DC converters including, but not limited to, the Silergy SY8101, SY8132, and SY8133 product families.

11. Upon information and belief, Silergy's acts of infringement have been with knowledge of the '643 Patent.

12. Upon information and belief, Silergy's infringement of the '643 Patent have been and continue to be willful.

13. Silergy's infringement of the '643 Patent has injured and damaged, and continue to injure and damage, MPS.

14. Silergy's infringement of the '643 Patent has caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

CLAIM II: INFRINGEMENT OF U.S. PATENT NO. 7,714,558

15. MPS incorporates by reference the allegations of paragraphs 1-14 above as fully set forth herein.

16. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 7,714,558 ("the '558 Patent") entitled "Short circuit current ratcheting in switch mode DC/DC voltage regulators," which was duly and legally issued by the United States Patent and Trademark Office on May 11, 2010. A copy of the'558 Patent is attached hereto as Exhibit B.

17. Silergy has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '558 Patent by making, using, offering to sell, selling, and/or other acts constituting infringement under 35 U.S.C. § 271 in the United States, including this judicial district, or importing into the United States, synchronous step-down DC/DC regulators including, but not limited to, the Silergy SY8033 product family.

18. Upon information and belief, Silergy's acts of infringement has been with knowledge of the '558 Patent.

19. Upon information and belief, Silergy's infringement of the '558 Patent has been and continues to be willful.

20. Silergy's infringement of the '558 Patent has injured and damaged, and continues to injure and damage, MPS.

21. Silergy's infringement of the '558 Patent has caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MPS prays that this Honorable Court enter judgment as follows:

1. That Silergy has infringed one or more claims of the '643 Patent;

2. That Silergy's infringement of the '643 Patent has been and/or is willful;

3. That Silergy has infringed one or more claims of the '558 Patent;

4. That Silergy's infringement of the '558 Patent has been and/or is willful;

5. That Silergy, and their respective agents, servants, officers, directors, employees, and all persons acting in concert with them directly or indirectly, be enjoined from infringing the '643 Patent and/or '558 Patent;

6. That Silergy be ordered to account for and pay to MPS damages arising out of Silergy's infringing activities, together with interest and costs, and all other damages permitted by 35 U.S.C. § 284, including enhanced damages up to three times the amount of damages found or measured;

7. That this action be adjudged an exceptional case and that MPS be awarded its attorneys' fees and costs in this action pursuant to 35 U.S.C § 285; and

8. That MPS be awarded such other equitable or legal relief as this Court deems just and proper under the circumstances.

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power Systems, Inc. demands a jury trial on all claims and issues so triable.

Dated: September 21, 2010

Respectfully submitted,
MONOLITHIC POWER SYSTEMS, INC.

By its attorneys,

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Exhibit 9

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CLERK U.S. DISTRICT COURT
CENTRAL DIST. OF CALIF.
LOS ANGELES

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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

CENTRAL DIVISION

Monolithic Power Systems, Inc., Plaintiff, v. Chip Advanced Technology Inc., Defendant.	Case No. CV07-08065 VBK VBKx **COMPLAINT FOR PATENT INFRINGEMENT** **DEMAND FOR JURY TRIAL** **FILE BY FAX**

Plaintiff Monolithic Power Systems, Inc. ("MPS") hereby pleads the following claim against Defendant Chip Advanced Technology Inc. ("CAT") and alleges as follows.

PARTIES

1. Plaintiff MPS is a California corporation having a principal place of business at 6409 Guadalupe Mines Road, San Jose, California 95120.

2. Defendant CAT is, upon information and belief, a corporation organized and existing under the laws of Taiwan, with a principal place of business at 3F, No. 1, JinShan 8th Street, HsinChu City, 300 Taiwan, but doing business throughout this judicial district and around the world.

JURISDICTION AND VENUE

3. This Court has subject matter jurisdiction over the action under 28 U.S.C. §§ 1331 and 1338(a) because the action concerns a federal question arising under the patent laws of the United States, including 35 U.S.C. § 271.

4. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(d) and 1400(b) because, among other reasons, CAT is subject to personal jurisdiction in this judicial district, has committed acts of infringement in this judicial district, and is an alien subject to suit in this judicial district.

5. Upon information and belief, CAT has placed infringing products into the stream of commerce by shipping those products into this judicial district (and other judicial districts) or knowing that such products would be shipped into this judicial district (and other judicial districts).

CLAIM FOR PATENT INFRINGEMENT

6. MPS incorporates by reference the allegations of paragraphs 1–5 above as fully set forth herein.

7. MPS is the owner by assignment of all right, title, and interest in and to United States Patent No. 6,897,643 ("the '643 patent") entitled "Integrated Circuit Driver Having Stable Bootstrap Power Supply," which was duly and legally issued by the United States Patent and Trademark on May 24, 2005. A copy of the '643 patent is attached hereto as Exhibit A.

8. CAT is directly infringing, contributing to the infringement of, or inducing others to infringe the '643 patent by making, using, offering to sell, or selling in the United States, or importing into the United States products that practice inventions claimed in the '643 patent.

9. Upon information and belief, CAT has had actual knowledge of the '643 patent.

10. Upon information and belief, CAT's infringement of the '643 patent has been willful.

11. CAT's past and continued acts of infringement have injured and damaged MPS.

12. CAT's acts of infringement have caused and will continue to cause irreparable injury to MPS unless and until enjoined by this Court.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MPS prays that this Court enter judgment as follows:

1. That CAT has infringed the '643 patent;

2. That CAT's infringement of the '643 patent is willful;

3. That CAT, and its respective agents, servants, officers, directors, employees, and all persons acting in concert with them directly or indirectly, be enjoined from infringing United States Patent No. 6,897,643;

4. That CAT be ordered to account for and pay to MPS the damages arising out of its infringing activities, together with interest and costs, and all other damages permitted by 35 U.S.C. § 284, including enhanced damages up to three times the amount of damages found or measured;

5. That this action be adjudged an exceptional case and that MPS be awarded its attorneys' fees, expenses and costs in this action pursuant to 35 U.S.C. § 285; and

6. That MPS be awarded such other equitable or legal relief as this Court deems just and proper under the circumstances.

Dated: December 10, 2007

FISH & RICHARDSON P.C.

By: _____
John P. Schnurer

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

DEMAND FOR JURY TRIAL

Plaintiff Monolithic Power Systems, Inc. demands a jury trial on all claims and issues.

Dated: December 10, 2007

FISH & RICHARDSON P.C.

By: _____
John P. Schnurer

Attorneys for Plaintiff
MONOLITHIC POWER SYSTEMS, INC.

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EXHIBIT A

US006897643B2

(12) **United States Patent**
Stone

(10) **Patent No.: US 6,897,643 B2**
(45) **Date of Patent: May 24, 2005**

(54) **INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY**

(75) Inventor: **Marshall David Stone**, Fremont, CA (US)

(73) Assignee: **Monolithic Power Systems, Inc.**, Los Gatos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 91 days.

(21) Appl. No.: **10/269,617**

(22) Filed: **Oct. 11, 2002**

(65) **Prior Publication Data**

US 2004/0070383 A1 Apr. 15, 2004

(51) **Int. Cl.**[7] **G05F 1/40**; H03K 17/60

(52) **U.S. Cl.** **323/288**; 323/224; 327/390; 327/589

(58) **Field of Search** 323/288, 224, 323/286, 282, 289, 225, 284, 285, 287; 363/60, 98, 17, 56, 132; 327/387, 390, 374–377, 434, 589, 537, 538, 536; 307/910, 475, 482, 578

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,883,978	A *	11/1989	Ohshima et al.	326/24
5,365,118	A	11/1994	Wilcox	
5,550,436	A	8/1996	Houk	
5,627,460	A *	5/1997	Bazinet et al.	323/288
5,828,262	A *	10/1998	Rees	327/390
6,172,493	B1 *	1/2001	Grant	323/288
6,462,522	B2 *	10/2002	Burstein et al.	323/282
6,661,208	B2 *	12/2003	Rutter et al.	323/224
2002/0036487	A1	3/2002	Moriconi et al.	

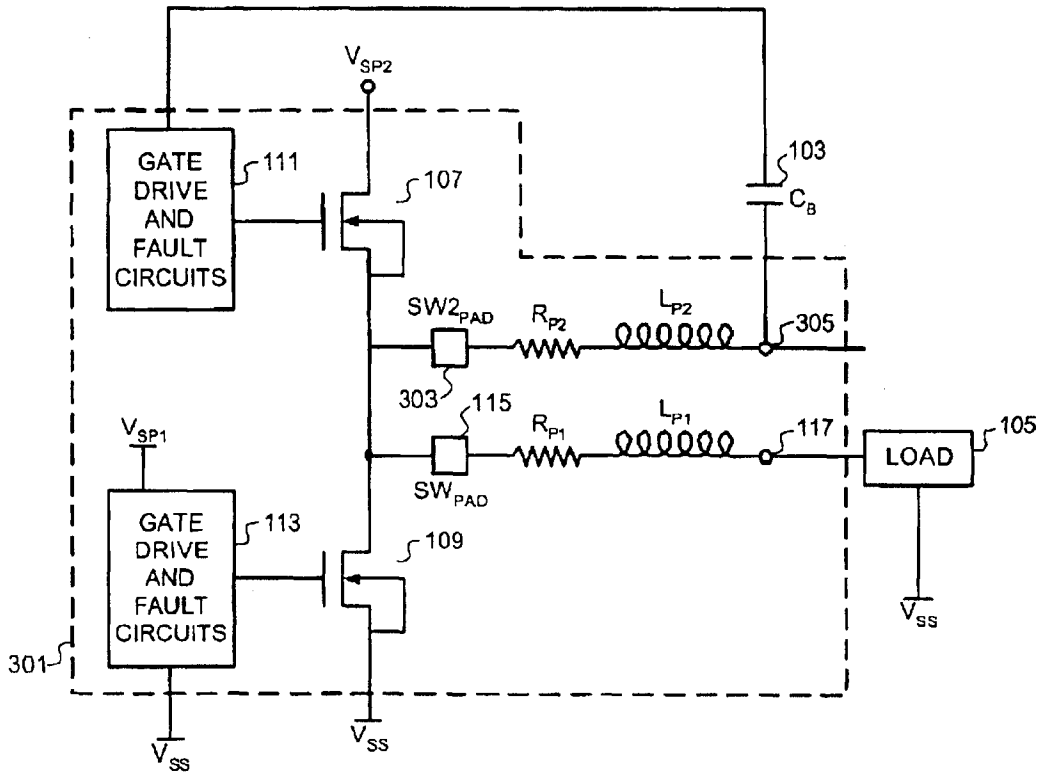
* cited by examiner

Primary Examiner—Rajnikant B. Patel
(74) *Attorney, Agent, or Firm*—Perkins Coie LLP

(57) **ABSTRACT**

An integrated circuit driver is disclosed. The driver comprises a high side transistor and a low side transistor connected in series. The output of the driver is taken from the source of the high side transistor and the drain of the low side transistor. A bootstrap contact pad is connected to the output node. Connected to the bootstrap contact pad is a bootstrap capacitor that is also connected to a high side gate drive that selectively controls the high side transistor.

14 Claims, 4 Drawing Sheets



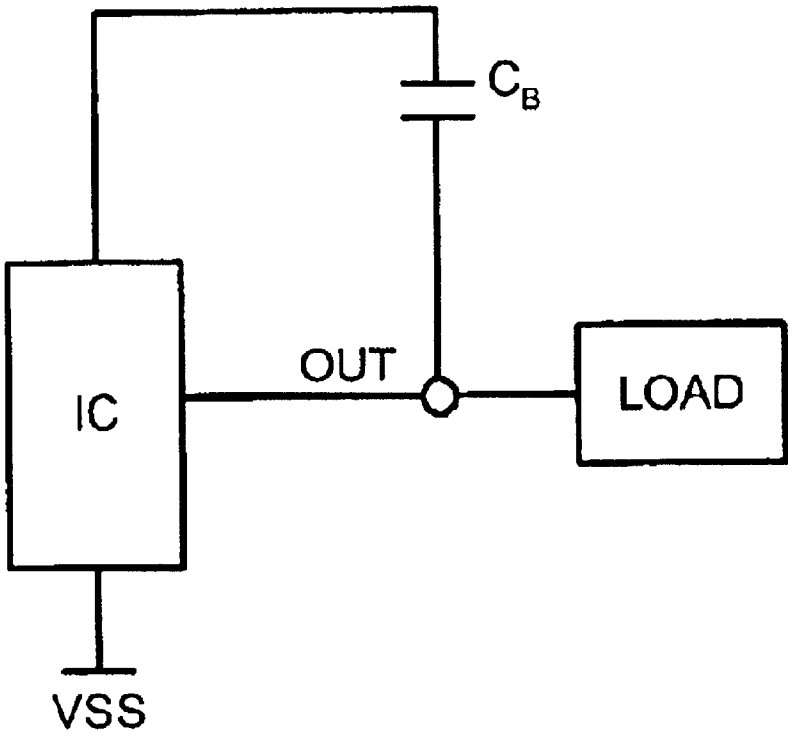


FIGURE 1
(PRIOR ART)

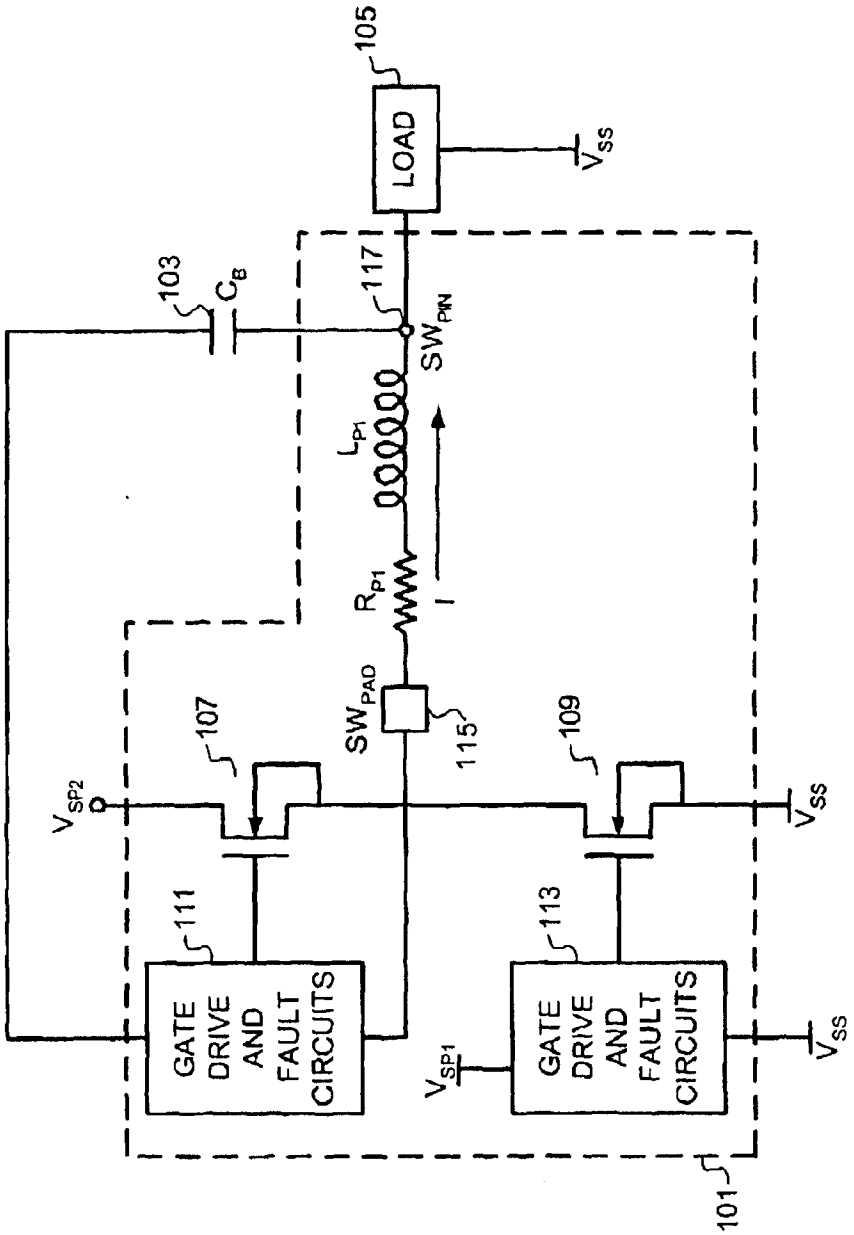
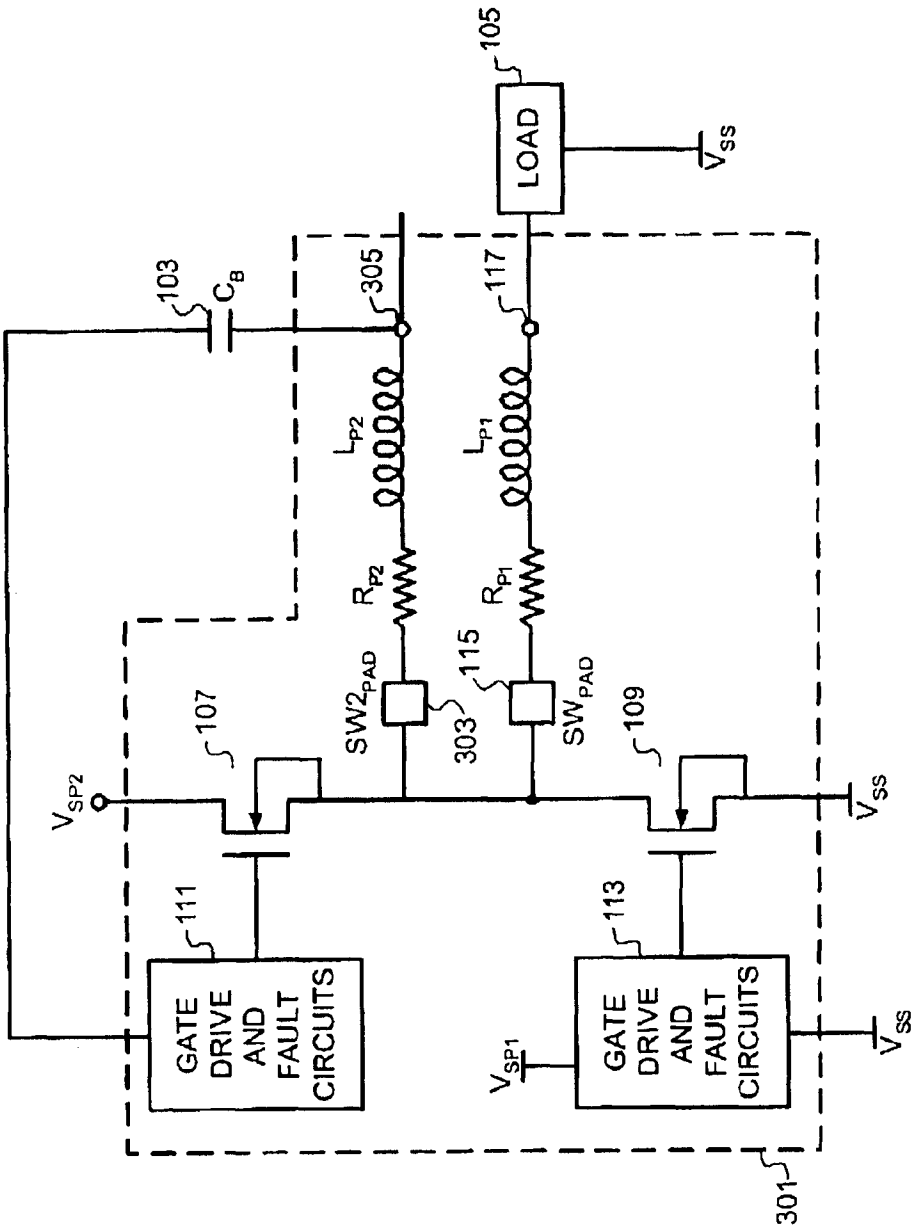


FIGURE 2
(PRIOR ART)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LOAD
V_{SS}
103
C_B
305
117
L_{P2}
L_{P1}
R_{P2}
R_{P1}
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115
303
SW_{PAD}
107
109
V_{SP2}
V_{SS}
111
113
GATE DRIVE AND FAULT CIRCUITS
GATE DRIVE AND FAULT CIRCUITS
V_{SP1}
V_{SS}
301

FIGURE 3

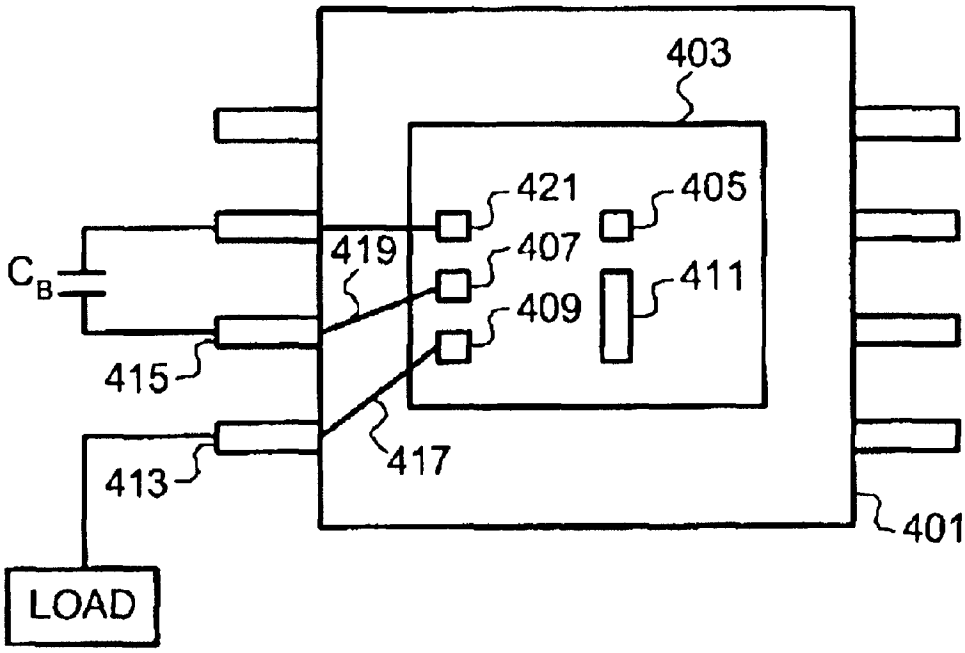

FIGURE 4

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Case 2:07-cv-08065-VBF-VBK Document 1 Filed 12/11/2007 Page 12 of 14

INTEGRATED CIRCUIT DRIVER HAVING STABLE BOOTSTRAP POWER SUPPLY

TECHNICAL FIELD

The present invention relates to integrated circuit drivers that use a bootstrap supply to drive the gate of the high side switch, and more particularly, to a method and apparatus for providing a stable bootstrap voltage to the gate of the high side switch.

BACKGROUND

One common type of integrated circuit driver utilizes two power MOSFET switches in a totem pole (half-bridge) topology. The MOSFET switches are typically NMOS switches that are connected in series. The power MOSFET switches are driven to conduct alternately. One of the MOSFET switches is designated as a high side switch, and the other MOSFET switch is designated as the low side switch. In one application, by selectively switching the power MOSFET switches in an alternating fashion, a load can be driven with an alternating current. In such a manner, a DC to AC inverter is formed. Likewise by controlling the switches according to an input signal (such as an acoustic signal), a class D audio amplifier is formed. Further, the same half bridge topology using a stable DC reference as the input can be used to create a DC power supply.

The gate of the high side switch is typically driven by a bootstrapped power supply. This is done to allow use of an NMOS switch, which has roughly half the on resistance of a PMOS switch of the same area. A bootstrap capacitor is used to increase the voltage available to the gate of the high side switch. FIG. **1** shows a prior art simplified schematic of an integrated circuit driver (IC) used in conjunction with a bootstrap capacitor to drive a load. The IC driver provides current to drive a load. A bootstrap capacitor C_b has one terminal connected to the output of the IC driver. The other terminal of the bootstrap capacitor C_b is provided back to the IC driver to drive the gate of the high side switch.

A more detailed schematic of the IC driver of FIG. **1** is shown in FIG. **2**. As seen in FIG. **2**, the IC driver **101** includes the high side switch **107** and the low side switch **109**. The high side switch **107** is driven by gate drive and fault circuit **111**. Similarly, the low side switch **109** is driven by gate drive and fault circuit **113**. The gate drive and fault circuits **111** and **113** are operative to control the switching of the high side and low side switches **107** and **109**. In addition, the gate drive and fault circuits **111** and **113** typically include fault detection circuitry and a bootstrap supply monitor. These additional functions are generally needed to measure whether there is a fault condition on the switch or whether the bootstrap supply is sufficient for the IC to operate properly.

The precise configuration of the gate drive and fault circuits **111** and **113** may be varied, but generally the configuration and operation is well known in the prior art. Note that the gate drive and fault circuit **113** used to control the low side switch **109** operates using a first supply voltage V_{sp1}. The low side switch **109** does not require a bootstrapped power supply. In contrast, the gate drive and fault circuit **111** that controls the high side switch **107** is connected to the bootstrap capacitor **103**.

The output of the IC driver **101** is taken from the node connecting the high side switch and the low side switch. In physical terms, the output node is a conductive pad on the integrated circuit, designated in FIG. **2** as SW_{pad} **115**. The integrated circuit die is then set into a package wherein the pad SW_{pad} **115** is connected to a package pin SW_{pin} **117**. The connection between the pad **115** and the package pin **117** is typically made through a bond wire formed of gold, copper, or other highly conductive material.

Nevertheless, the bond wire between the pad **115** and the package pin **117** includes some finite amount of parasitic inductance L_{p1} and parasitic resistance R_{p1}. When current is supplied through the pin **117** to the load **105**, invariably there will be a loss of voltage across the parasitic inductance L_{p1} and parasitic resistance R_{p1}.

The amount of the voltage drop is important because any voltage that develops across the bond wire between SW pad and SW pin, subtracts directly and instantaneously from the bootstrap supply. Because of the large value of current and high rate of change of that current in the bondwire, the voltage drop can be significant, on the order of two or more volts. This sudden drop in the internal bootstrap supply voltage will adversely affect any signal processing operating under the internal bootstrap supply, such as the bootstrap supply monitor and fault check circuits.

Therefore, the arrangement shown in FIG. **2** having an imprecise and noisy bootstrap supply is undesirable.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram showing a bootstrap capacitor and an integrated circuit driver for driving a load.

FIG. **2** is a detailed schematic of the integrated circuit driver of FIG. **1**.

FIG. **3** is a schematic circuit diagram illustrating one embodiment of the present invention.

FIG. **4** is an illustration of an integrated circuit die mounted on an integrated circuit package.

DETAILED DESCRIPTION

The present invention is an integrated circuit driver having a "quieter" bootstrap power supply. The integrated circuit driver has an output pin and output pad that is dedicated to the bootstrap capacitor thereby maintaining a stable bootstrap supply voltage. In the following description, some specific details, such as example values for the circuit components, are provided to provide a thorough understanding of embodiments of the invention. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

Reference throughout this specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments. One skilled in the relevant art will recognize, however, that the invention can be practiced without one or more of the specific details, or with other methods, components, materials, etc. In other instances, well-known structures, materials, or operations are not shown or described in detail to avoid obscuring aspects of the invention.

FIG. **3** shows one embodiment of the present invention. As seen, FIG. **3** is substantially similar to the prior art IC driver **101**, except that an additional pad $SW2_{pad}$ **303** is also attached to the output node between the high side switch **107** and the low side switch **109**. Additionally, a second output pin **305** is provided from the IC driver **301**. Having the second pad **303** and the second package pin **305** connected to the bootstrap capacitor **103**, the bootstrap capacitor **103** is not affected by any voltage drop caused by current flowing to the load **105** through a first package pin **117**.

Note that substantially all the current provided by the high side switch **107** and the low side switch **109** flows to the load **105** through the package pin **117**. Little if any current flows through the second package pin **305**, thereby eliminating any voltage drop through the parasitic resistance and inductance of the bond wire connecting the second package pin **305** to the second pad **303**. Thus, the bootstrap supply voltage provided by the bootstrap capacitor **103** maintains its value and is less noisy.

As seen, the IC driver **301** of the present invention includes an additional package pin **305** that is connected directly to the bootstrap capacitor **103**. In an alternative embodiment, the second package pin **305** has a bond wire directly attached to the same pad **115** as the first package pin **117**. This saves the requirement for forming the second pad **303**. In one embodiment, the IC driver **301** may be used to drive, for example, a cold-cathode fluorescent lamp. However, typically, the lamp is connected through a secondary winding of a transformer whose primary winding is connected to the output of the IC driver **301**.

FIG. **4** further illustrates the arrangement of the present invention. In FIG. **4**, an integrated circuit package **401** is adapted to mount an integrated circuit die **403**. The integrated circuit die **403** includes various circuitry, such as the low side switch, the high side switch, and the gate drive and fault circuitry. In addition, the integrated circuit die **403** includes an output contact pad **409**, a bootstrap contact pad **407** (referred to as a second pad $SW2_{pad}$ **303** in FIG. **3**), a high side gate drive input pad **421**, and various other contact pads **405** and **411**.

The output contact pad **409** is connected to an output pin **413** of the integrated circuit package **401** by an output bond wire **417**. The output bond wire **417** is secured to the output pin **413** and the output contact pad **409**. The bootstrap contact pad **407** is connected to bootstrap pin **415** of the integrated circuit package **401** by a bootstrap bond wire **419**. The bootstrap bond wire **419** is secured to the bootstrap pin **415** and the bootstrap contact pad **407**.

The bootstrap capacitor C_b is connected between the bootstrap pin **415** and the gate drive circuitry on the integrated circuit **403** through another package pin and high side gate drive input pad **421**. Finally, the load is connected to the output pin **413**. The other various pins of the integrated circuit package **401** are used in known configurations, such as for power supply, ground, control lines, and such.

As noted above, in an alternate embodiment, the output contact pad **409** and the bootstrap contact pad **407** is one and the same. Whichever pad conducts current to the load is made large, such as contact pad **411**, but not changed in size if also attached to Cb.

Thus, the above described IC driver provides a stable bootstrap power supply, even when large amounts of power are being delivered. This is accomplished by connecting the bootstrap capacitor to a dedicated bootstrap pin and contact pad.

From the foregoing, it will be appreciated that specific embodiments of the invention have been described herein for purposes of illustration, but that various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a bootstrap contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap contact pad, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output contact pad connected to the output node, said output contact pad providing an output signal to a load.

2. The driver of claim **1** wherein said high side transistor and said low side transistor are NMOS transistors.

3. The driver of claim **1** wherein said output contact pad and said bootstrap contact pad are the same.

4. The driver of claim **1** further including an output package pin connected to said output pad by an output bond wire.

5. The driver of claim **1** further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

6. The driver of claim **3** further including an output package pin connected to said output pad by an output bond wire.

7. The driver of claim **3** further including a bootstrap package pin connection to said bootstrap contact pad by a bootstrap bond wire.

8. An integrated circuit package comprising:

(a) an integrated circuit die, said die having formed thereon:

(1) a high side transistor;

(2) a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

(3) a set of two bootstrap contact pads connected to the output node;

(4) a high side gate drive for selectively controlling the high side transistor;

(5) a low side gate drive for selectively controlling the low side transistor; and

(6) a set of two output contact pads connected to the output node, said output contact pads providing output signals to a load;

(b) a set of two carrier packages having a plurality of package pins including at least a bootstrap package pin and an output package pin, said carrier packages for securing said integrated circuit die;

(c) a set of two output bond wires connecting said output contact pads with said output package pins; and

(d) a set of two bootstrap bond wires connecting said bootstrap contact pads with said bootstrap package pins.

9. The package of claim **8** wherein said high side transistor and said low side transistor are NMOS transistors.

10. The package of claim **8** wherein said output contact pad and said bootstrap contact pad are the same.

11. The package of claim **8** wherein a first terminal of a bootstrap capacitor is connected to said bootstrap package pin and a second terminal of said bootstrap capacitor is connected to an input to said high side gate drive.

12. A method for driving a load using a high side switch and a low side switch connected in series, the source of said high side switch connected to the drain of said low side switch, the connection of said high side switch and said low side switch being an output node, the method comprising:

providing a bootstrap contact pad connected to said output node;

providing an output pad connected to said output node;

connecting a bootstrap capacitor to said bootstrap contact pad, said bootstrap capacitor used to provide a bootstrap power supply to a gate drive of said high side switch, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor; and

connecting said output pad to said load.

13. An integrated circuit driver comprising:

a high side transistor;

a low side transistor connected in series to said high side transistor such that the source of said high side transistor is connected to the drain of said low side transistor, the source of the high side transistor and the drain of the low side transistor forming an output node;

a combination bootstrap/output contact pad connected to the output node;

a bootstrap capacitor having a first terminal connected to said bootstrap/output contact pad via a bootstrap capacitor package pin, wherein the bootstrap capacitor couples to the gate and the source of the high side transistor;

a high side gate drive for selectively controlling the high side transistor, said high side gate drive having as an input a signal from a second terminal of said bootstrap capacitor;

a low side gate drive for selectively controlling the low side transistor; and

an output package pin connecting said bootstrap/output contact pad to a load.

14. The driver of claim **13** wherein said high side transistor and said low side transistor are NMOS transistors.

* * * * *

Exhibit 10

FILED
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RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

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by
Wheels of Justice

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

C 08 4567 JL

MONOLITHIC POWER SYSTEMS, INC., Plaintiff, v. O2MICRO INTERNATIONAL LIMITED, Defendant.	Case No. **COMPLAINT FOR DECLARATORY JUDGMENT** **DEMAND FOR JURY TRIAL**

Plaintiff Monolithic Power Systems, Inc. ("MPS") hereby pleads the following claims for Declaratory Judgment against Defendant O2Micro International Limited ("O2Micro"), and allege as follows.

PARTIES

1. Plaintiff MPS is a corporation organized under the laws of the State of Delaware with its principal place of business located at 6409 Guadalupe Mines Road, San Jose, California 95120.

2. On information and belief, Defendant O2Micro is a corporation organized under the laws of the Cayman Islands with its principal place of business located at The Grand Pavilion,

West Bay Road, PO Box 32331 SMB George Town, Grand Cayman, Cayman Islands, but doing business throughout this judicial district and around the world.

JURISDICTION AND VENUE

3. The Court has subject matter jurisdiction over this action and the matters pleaded herein under 28 U.S.C. §§ 1331 and 1338(a) because the action arises under the Federal Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, and the Patent Act of the United States, 35 U.S.C. § 101, *et seq*.

4. Venue is proper in this judicial district pursuant to 28 U.S.C. § 1391(d) because O2Micro is an alien corporation organized under the laws of the Cayman Islands subject to suit in this judicial district.

INTRADISTRICT ASSIGNMENT

5. This action for a declaratory judgment of non-infringement and invalidity of patents is assigned on a district-wide basis under Civil L.R. 3-2(c).

GENERAL ALLEGATIONS

6. This action involves U.S. Patent No. 6,856,519 ("the '519 patent"), attached hereto as Exhibit A; U.S. Patent No. 6,809,938 ("the '938 patent") attached hereto as Exhibit B; U.S. Patent No. 6,900,993 ("the '993 patent") attached hereto as Exhibit C; and U.S. Patent No. 7,120,035 ("the '035 patent") attached hereto as Exhibit D (collectively "the patents in suit"). The '938, '993, and '035 patents are a division of the '519 patent; all of the patents in suit are directed to multifunctional/multitasked pin technologies.

7. MPS has developed power inverter controller products, including the inverter controller MP1009, without knowledge of any of the patents in suit.

8. Separately on July 31, 2008 and September 17, 2008, O2Micro telephoned MPS's customer Innolux Display Corporation ("Innolux"), alleging that MPS's inverter controller product MP1009 ("MP1009 inverter controller") infringed the multifunctional/multitasked pin related patents of O2Micro and that O2Micro planned on instituting a lawsuit against MPS on those patents.

9. Upon information and belief, O2Micro contends that MP1009 inverter controller, and devices incorporating these products, infringe one or more claims of the patents in suit and that those claims are valid.

10. MPS denies that the MP1009 inverter controller or any of MPS's products infringe any claim of the patents in suit, and also denies that these patents are valid.

FIRST CLAIM FOR RELIEF

Declaratory Relief Regarding Non-Infringement

11. MPS incorporates herein the allegations of paragraphs 1-10.

12. An actual and justiciable controversy exists between Plaintiff MPS and Defendant O2Micro as to non-infringement of the patents in suit, which is evidenced by O2Micro's repeated assertions communicated to Innolux that MPS's MP1009 inverter controller infringes valid claims of the patents in suit, and MPS's allegations herein.

13. Pursuant to the Federal Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, MPS requests the declaration of the Court that MPS does not infringe and has not infringed any claim of the patents in suit.

SECOND CLAIM FOR RELIEF

Declaratory Relief Regarding Invalidity

14. MPS incorporates herein the allegations of paragraphs 1-10.

15. An actual and justiciable controversy exists between Plaintiff MPS and Defendant O2Micro as to invalidity of the patents in suit, which is evidenced by O2Micro's repeated assertions communicated to Innolux that MPS's MP1009 inverter controller infringes valid claims of the patents in suit, and MPS's allegations herein..

16. Pursuant to the Federal Declaratory Judgment Act, 28 U.S.C. § 2201 *et seq.*, MPS requests the declaration of the Court that the patents in suit are invalid under the Patent Act, 35 U.S.C. § 101, *et seq.*, including, but not limited to, sections 102, 103 and 112.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff MPS prays that the Court enter declaratory judgment as follows:

(1) That MPS does not infringe and has not infringed, directly or indirectly, any of the patents in suit;

(2) That the patents in suit are invalid;

(3) That O2Micro, and all persons acting on its behalf or in concert with it, be permanently enjoined and restrained from charging, orally or in writing, that any of the patents in suit is infringed by MPS, directly or indirectly.

(4) That MPS be awarded its costs, expenses and reasonable attorney fees in this action; and

(5) That MPS be awarded such other and further relief as the Court may deem appropriate.

DEMAND FOR JURY TRIAL

Plaintiff MPS hereby demands a jury trial in this action.

DATED: September 30, 2008

FISH & RICHARDSON P.C.

By: John P. Schnurer

Attorneys for Plaintiff
Monolithic Power Systems, Inc.

EXHIBIT A

US006856519B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.: US 6,856,519 B2**
(45) **Date of Patent: Feb. 15, 2005**

(54) **INVERTER CONTROLLER**

(75) Inventors: **Yung-Lin Lin**, Palo Alto, CA (US); **Da Liu**, San Jose, CA (US)

(73) Assignee: **O2Micro International Limited**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 76 days.

(21) Appl. No.: **10/139,619**

(22) Filed: **May 6, 2002**

(65) **Prior Publication Data**

US 2003/0206426 A1 Nov. 6, 2003

(51) **Int. Cl.**[7] **H02M 3/335**

(52) **U.S. Cl.** **363/16**; 363/132; 315/307; 323/905

(58) **Field of Search** 345/204, 205, 345/208, 210, 211, 212; 315/306, 307; 363/25, 16, 17, 132; 713/1; 323/905

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,277,728 A	7/1981	Stevens	315/307
4,504,895 A	3/1985	Steigerwald	363/17
4,535,399 A	8/1985	Szepesi	363/20
4,541,041 A	9/1985	Park et al.	363/41
4,672,528 A	6/1987	Park et al.	363/98
4,727,469 A	2/1988	Kammiller	363/56
4,752,700 A	6/1988	Boyacigiller	307/297
4,794,506 A	12/1988	Hino et al.	363/17
4,814,962 A	3/1989	Magalhaes et al.	363/16
4,833,584 A	5/1989	Divan	363/37
4,855,888 A	8/1989	Henze et al.	363/132
4,860,189 A	8/1989	Hitchcock	363/132
4,864,483 A	9/1989	Divan	363/37
4,912,622 A	3/1990	Steigerwald et al.	363/98
4,935,857 A	6/1990	Nguyen et al.	363/17
4,952,849 A	8/1990	Fellows et al.	315/307
4,953,068 A	8/1990	Henze	363/17
4,988,920 A	1/1991	Hoeksma	315/101
4,992,919 A	2/1991	Lee et al.	363/17

(List continued on next page.)

OTHER PUBLICATIONS

"Introduction to the Principles and Features of Resonant Power Conversion", Steve Freeland, from *Recent Developments in Resonant Power Conversion*, Intertec Communications, Inc., 1988, 20–43, no month.

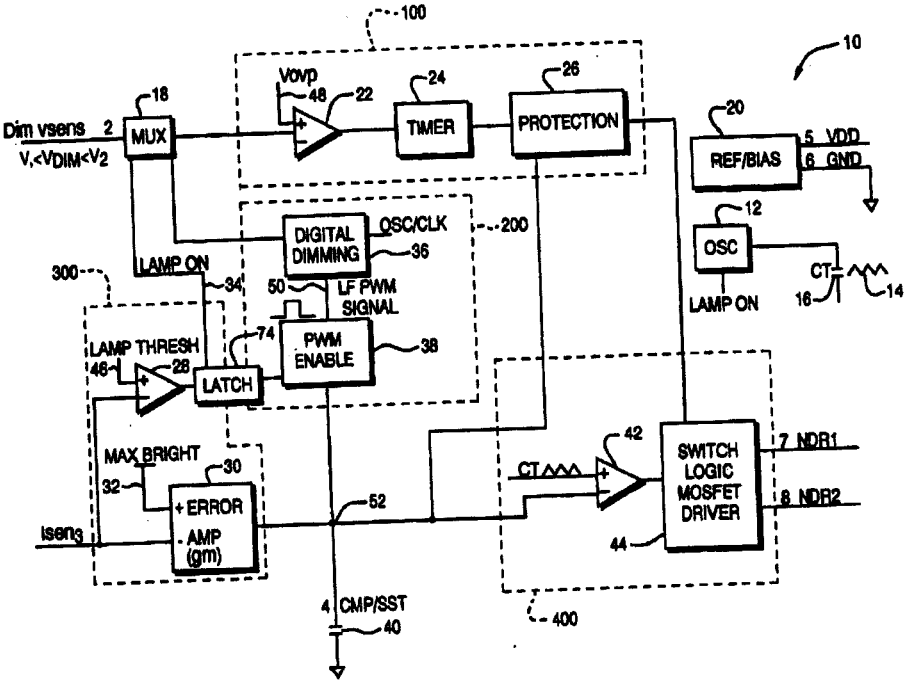
(List continued on next page.)

Primary Examiner—Jessica Han
(74) *Attorney, Agent, or Firm*—Grossman, Tucker, Perreault & Pfleger, PLLC

(57) **ABSTRACT**

An integrated circuit inverter controller that includes at least one input pin that is configured to receive two or more input signals. The input pin may be multiplexed so that the appropriate input signal is directed to appropriate circuitry within the controller to support two or more functions of the controller. Alternatively, the input signals may be present in differing time periods so that a single pin can support two or more functions. Multifunctional or multitasked pins reduce the overall pin count of the inverter controller.

7 Claims, 6 Drawing Sheets



U.S. PATENT DOCUMENTS

5,017,800	A	5/1991	Divan	307/66
5,027,263	A	6/1991	Harada et al.	363/16
5,027,264	A	6/1991	DeDoncker et al.	363/16
5,105,127	A	4/1992	Lavaud et al.	315/291
5,113,334	A	5/1992	Tuson et al.	363/25
5,132,888	A	7/1992	Lo et al.	363/17
5,132,889	A	7/1992	Hitchcock et al.	363/17
5,157,592	A	10/1992	Walters	363/17
5,166,579	A	11/1992	Kawabata et al.	315/209
5,198,969	A	3/1993	Redl et al.	363/17
5,208,740	A	5/1993	Ehsani	363/124
5,231,563	A	7/1993	Jitaru	363/98
5,235,501	A	8/1993	Stuart et al.	363/17
5,268,830	A	12/1993	Loftus, Jr.	363/17
5,270,620	A	12/1993	Basch et al.	315/291
5,285,372	A	2/1994	Huynh et al.	363/132
5,291,382	A	3/1994	Cohen	363/16
5,305,191	A	4/1994	Loftus, Jr.	363/17
5,311,104	A	5/1994	Antle	315/307
5,363,020	A	11/1994	Chen et al.	315/209 R
5,384,516	A	1/1995	Kawabata et al.	315/160
5,402,043	A	3/1995	Nilssen	315/307
5,402,329	A	3/1995	Wittenbreder, Jr.	363/16
5,412,557	A	5/1995	Lauw	363/37
5,418,703	A	5/1995	Hitchcock et al.	363/17
5,420,779	A	5/1995	Payne	363/56
5,422,546	A	6/1995	Nilssen	315/219
5,430,632	A	7/1995	Meszlenyi	363/17
5,430,641	A	7/1995	Kates	363/133
5,438,497	A	8/1995	Jain	363/17
5,438,498	A	8/1995	Ingemi	363/17
5,442,540	A	8/1995	Hua et al.	363/98
5,448,155	A	9/1995	Jutras	323/285
5,448,467	A	9/1995	Ferreira	363/17
5,477,131	A	12/1995	Gegner	323/222
5,481,160	A	1/1996	Nilssen	315/209 R
5,481,449	A	1/1996	Kheraluwala et al.	363/17
5,510,974	A	4/1996	Gu et al.	363/134
5,514,921	A	5/1996	Steigerwald	307/125
5,546,300	A	8/1996	Lee et al.	363/132
5,550,436	A	8/1996	Houk	315/209
5,559,688	A	9/1996	Pringle	363/89
5,583,402	A	12/1996	Moisin et al.	315/307
5,604,411	A	2/1997	Venkitasubrahmanian et al.	315/307
5,615,093	A *	3/1997	Nalbant	363/25
5,619,402	A	4/1997	Liu	363/20
5,638,260	A	6/1997	Bees	363/17
5,642,065	A	6/1997	Choi et al.	327/110
5,646,836	A	7/1997	Sadarnac et al.	363/98
5,669,238	A	9/1997	Devers	62/657
5,677,602	A	10/1997	Paul et al.	315/224
5,684,683	A	11/1997	Divan et al.	33/65
5,694,007	A	12/1997	Chen	315/247
5,712,533	A	1/1998	Corti	315/169.3
5,715,155	A	2/1998	Shahani et al.	363/132
5,719,474	A	2/1998	Vitello	315/307
5,731,652	A	3/1998	Shimada	310/316
5,736,842	A	4/1998	Jovanovic	323/222
5,742,495	A	4/1998	Barone	363/65
5,742,496	A	4/1998	Tsutsumi	363/95
5,744,915	A	4/1998	Nilssen	315/209 R
5,748,457	A	5/1998	Poon et al.	363/16
5,754,012	A	5/1998	LoCascio et al.	315/307
5,764,494	A	6/1998	Schutten et al.	363/17
5,774,346	A	6/1998	Poon et al.	363/17
5,781,418	A	7/1998	Chang et al.	363/16
5,781,419	A	7/1998	Kutkut et al.	363/17
5,784,266	A	7/1998	Chen	363/16
5,796,598	A	8/1998	Nowak et al.	363/37
5,818,172	A	10/1998	Lee	315/86
5,834,889	A	11/1998	Ge	313/493
5,844,540	A	12/1998	Terasaki	345/102
5,854,617	A	12/1998	Lee et al.	345/102
5,856,916	A	1/1999	Bonnet	363/20
5,875,103	A	2/1999	Bhagwat et al.	363/17
5,880,940	A	3/1999	Poon	363/20
5,886,477	A	3/1999	Honbo et al.	315/209 PZ
5,886,884	A	3/1999	Baek et al.	363/48
5,894,412	A	4/1999	Faulk	363/56
5,910,709	A	6/1999	Stevanovic et al.	315/225
5,917,722	A	6/1999	Singh	363/132
5,923,129	A	7/1999	Henry	315/307
5,930,121	A	7/1999	Henry	363/16
5,932,976	A	8/1999	Maheshwari et al.	315/291
5,939,830	A	8/1999	Praiswater	315/DIG. 4
5,946,200	A	8/1999	Kim et al.	363/17
6,002,210	A	12/1999	Nilssen	315/219
6,011,360	A	1/2000	Gradzki et al.	315/244
6,016,052	A	1/2000	Vaughn	323/355
6,114,814	A	9/2000	Shannon et al.	315/219
6,198,236	B1 *	3/2001	O'Neill	315/307
6,316,881	B1	11/2001	Shannon et al.	315/219
6,396,722	B2	5/2002	Lin	363/98
6,640,271	B2 *	10/2003	Ehrenhardt et al.	710/100

OTHER PUBLICATIONS

"Zero–Voltage Switching Technique in DC/DC Converters", Kwang–Hwa Liu and Fred C. Lee, from *Recent Developments in Resonant Power Convertion*, Intertec Communications, Inc., 1988, pp. 211–223, no month.

"A New and Improved Control Technique Greatly Simplifies the Design of ZVS Resonant Inverters and DC/DC Power Supplies", Mehmet K. Nalbant, 1995 IEEE, pp. 694–701, no month.

Switching Power Supply Design, Abraham I. Pressman, McGraw–Hill, 1991, pp. 93–104; 471–492, no month.

"Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller", by Bill Andreycak, Unitrode, Application Note, May 1997, pp. 1–14.

"Fixed–Frequency, Resonant–Switched Pulse Width Modulation with Phase–Shifted Control", by Bob Mammano and Jeff Putsch, from *Power Supply Design Seminar*, Unitrode, 1991, pp. 5–1 to 5–7, no month.

"Zero Voltage Switching Resonant Power Conversion", by Bill Andreycak, from *Power Supply Design Seminar*, Unitrode, 1991, pp. A2–1 to A2–24; and A2–1A to A2–A3, no month.

"Resonant Mode Converter Topologies", Bob Mammano, from *Power Supply Design Seminar*, Unitrode, 1991, pp. P3–1 to P3–12, no month.

"The New UC3879 Phase–Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full–Bridge Converters", by Laszo Balogh, Unitrode, Application Note, 1995, pp. 1–8, no month.

"A Comparative Study of a Class of Full Bridge Zero–Voltage–Switched PWM Converters", by W. Chen et al., 1995 IEEE, pp. 893–899, no month.

"Optimum ZVS Full–Bridge DC/DC Converter with PWM Phase–Shift Control: Analysis, Design Considerations, and Experimental Results", by Richard Red I et al., 1994 IEEE, pp. 159–165, no month.

"A Frequency/PWM Controlled Converter with Two Independently Regulated Outputs", by R.A. Fisher et al., HFPC, May 1989, pp. 459–471.
"Feasible Characteristic Evaluations of Resonant Tank PWM Inverter–Linked DC–DC High–Power Converters for Medical–Use High–Voltage Application", by H. Takano et al., 1995 IEEE, pp. 913–919, no month .
"High Density Power–Hybrid Design of a Half–Bridge Multi–Resonant Converter", by Richard Farrington, et al., HFPC–Virginia Polytechnic Institute, May 1990, pp. 26–33.
"Small–Signal Analysis of the Zero–Voltage Switched Full–Bridge PWM Converter", by V. Vlatkovic et al., HFPC–virginia Polytechnic Institute, May 1990, pp. 262–272.
Melvin C. Cosby, Jr. & R. M. Nelms, "A Resonant Inverter for Electronic Ballast Applications," IEEE Transactions on Industrial Electronics, vol. 41, No. 4, pp. 418–425 (Aug. 1994).
Steigerwald, "A Comparison of Half–Bridge Resonant Converter Topologies," IEEE Transactions on Power Electronics, vol. 3, No. 2, pp. 174–182 (Apr. 1998).
M.A. Cayless and A.M. Marsden, "Lamps and Lighting", Third Edition, Thorn EMI Lighting Ltd 1983, pp. 322–323, no month.
"BiCMOS Cold Cathode Fluorescent Lamp Driver Controller", Unitrode Products, Texas Instruments, Oct. 1998, Revised Nov. 2000.
* cited by examiner

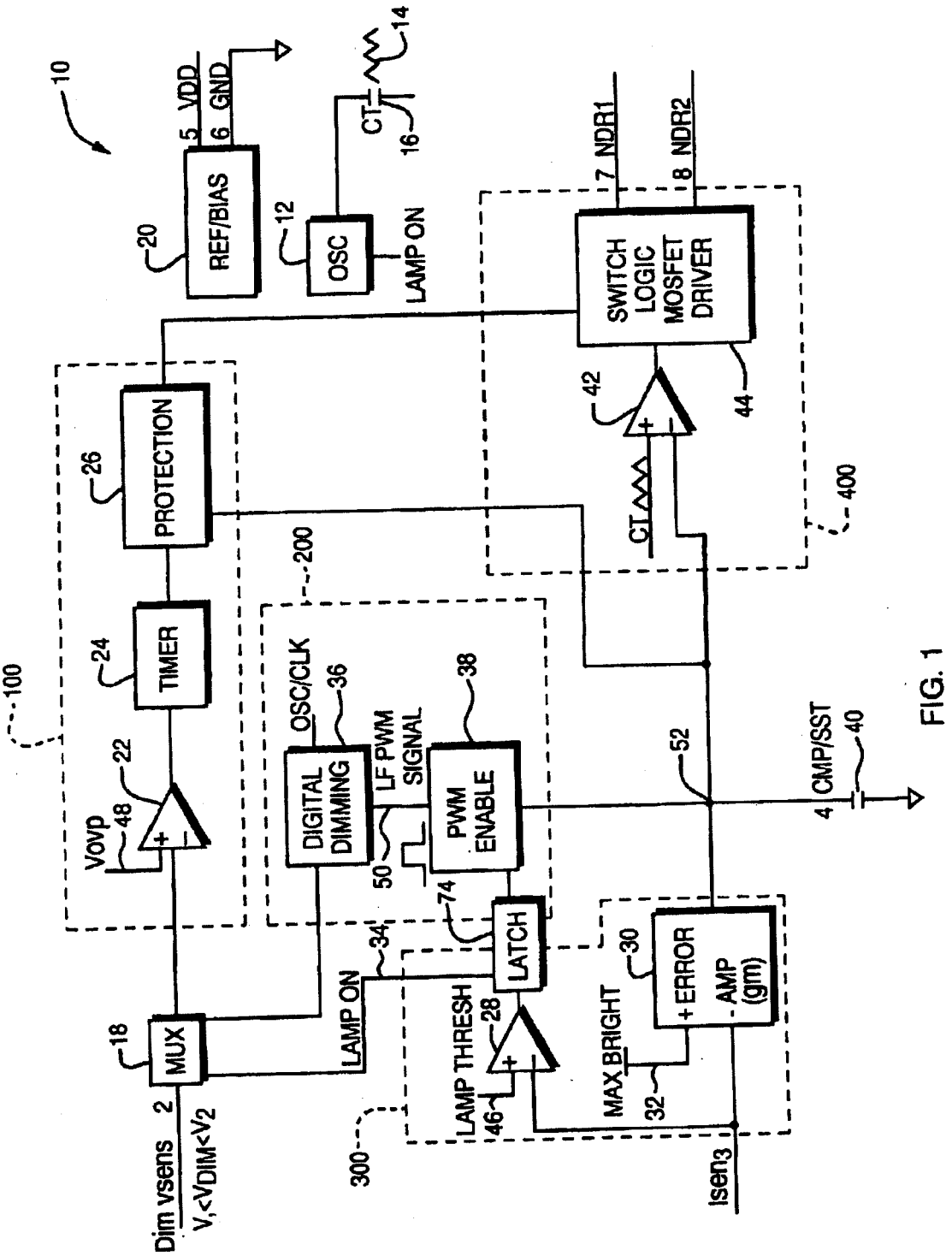

10
5 VDD
6 GND
REF/BIAS
20
OSC
12
CT
16
14
LAMP ON
7 NDR1
8 NDR2
SWITCH LOGIC MOSFET DRIVER
42
44
PROTECTION
26
CT
400
200
100
TIMER
24
OSC/CLK
36
DIGITAL DIMMING
LF PWM SIGNAL
38
PWM ENABLE
52
CMP/SST
40
4
22
Vovp
48
50
74
LATCH
34
LAMP ON
18
MUX
LAMP THRESH
28
MAX BRIGHT
30
+ ERROR AMP (gm) -
32
46
300
Dim vsens 2
V,<VDIM<V2
Isen3

FIG. 1

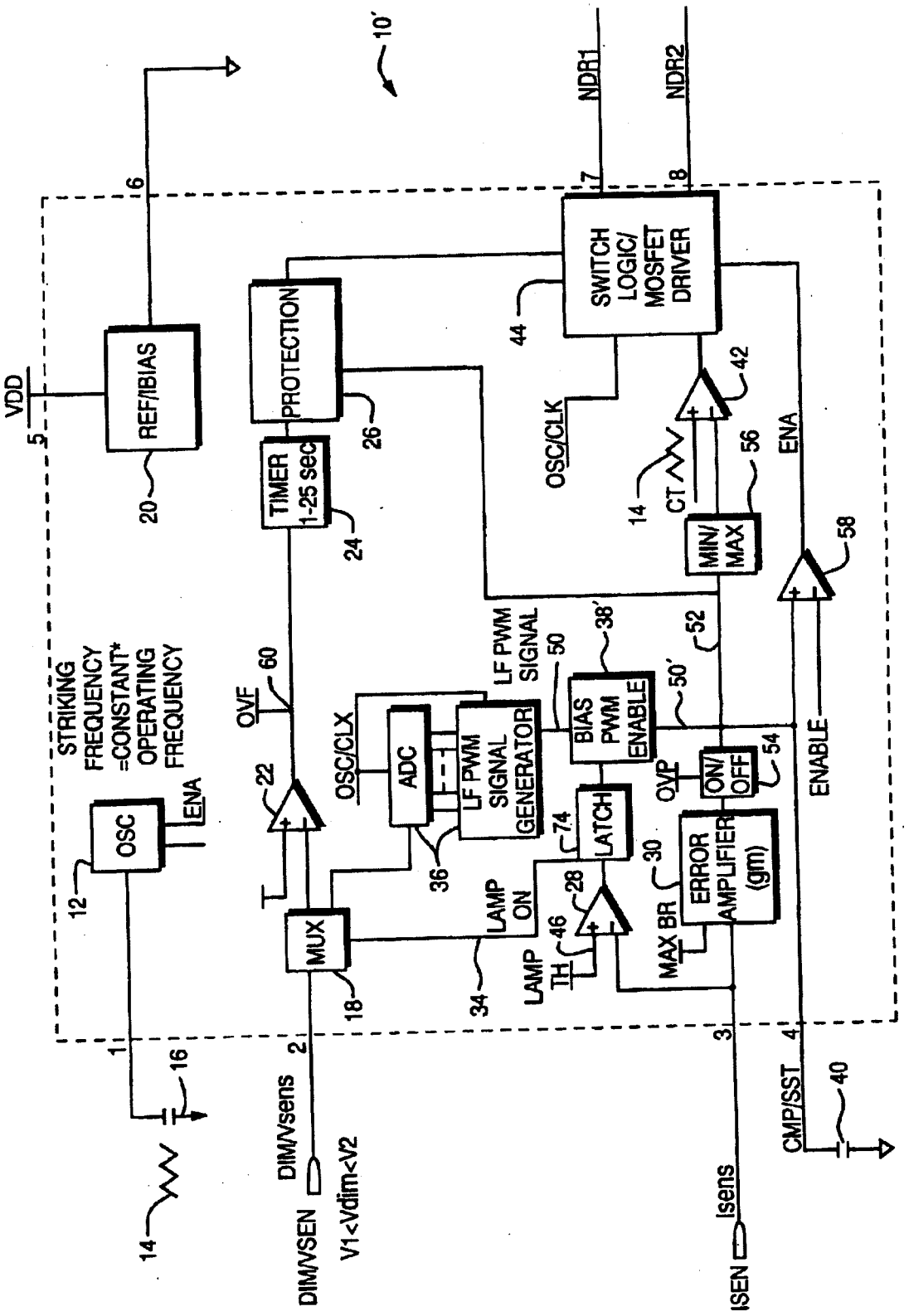

10'
NDR1
NDR2
VDD
5
6
7
8
REF/IBIAS
20
PROTECTION
26
TIMER 1-25 sec
24
SWITCH LOGIC/ MOSFET DRIVER
44
42
OSC/CLK
CT
14
56
MIN/ MAX
ENA
58
LF PWM SIGNAL
50
38'
52
50'
BIAS PWM ENABLE
OVF
60
OSC/CLK
ADC
LF PWM SIGNAL GENERATOR
22
OVP
ON/ OFF
54
ENABLE
STRIKING FREQUENCY =CONSTANT* OPERATING FREQUENCY
OSC
ENA
12
74
LATCH
ERROR AMPLIFIER (gm)
30
36
LAMP ON
28
MAX BR
46
LAMP TH
MUX
18
34
1
2
3
4
16
CMP/SST
40
DIM/Vsens
V1<Vdim<V2
DIM/VSEN
Isens
ISEN
14

FIG. 2

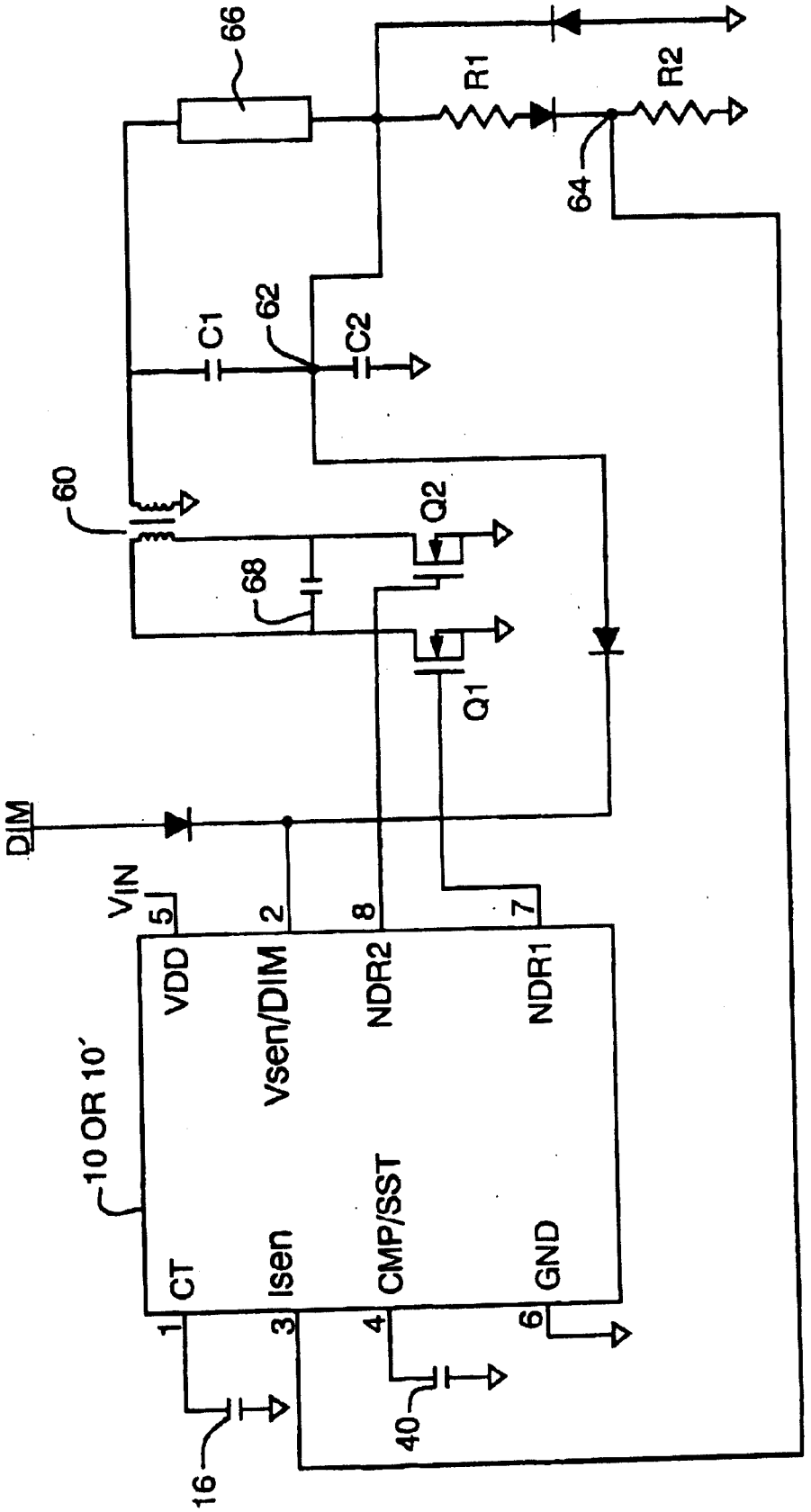

66
R1
R2
64
C1
62
C2
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen/DIM
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
16
40

FIG. 3

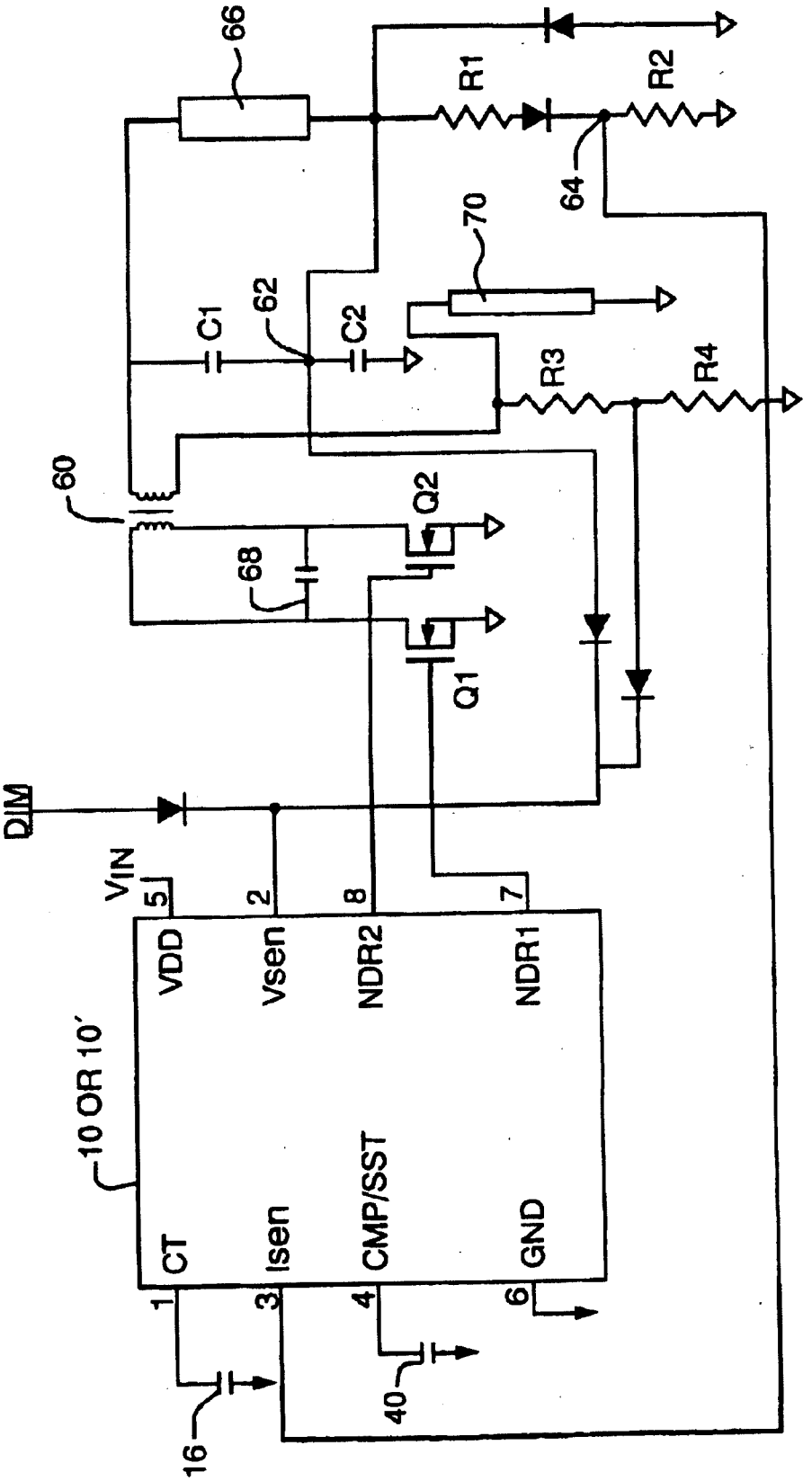

66
R1
R2
64
70
62
C1
C2
R3
R4
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
16
40

FIG. 4

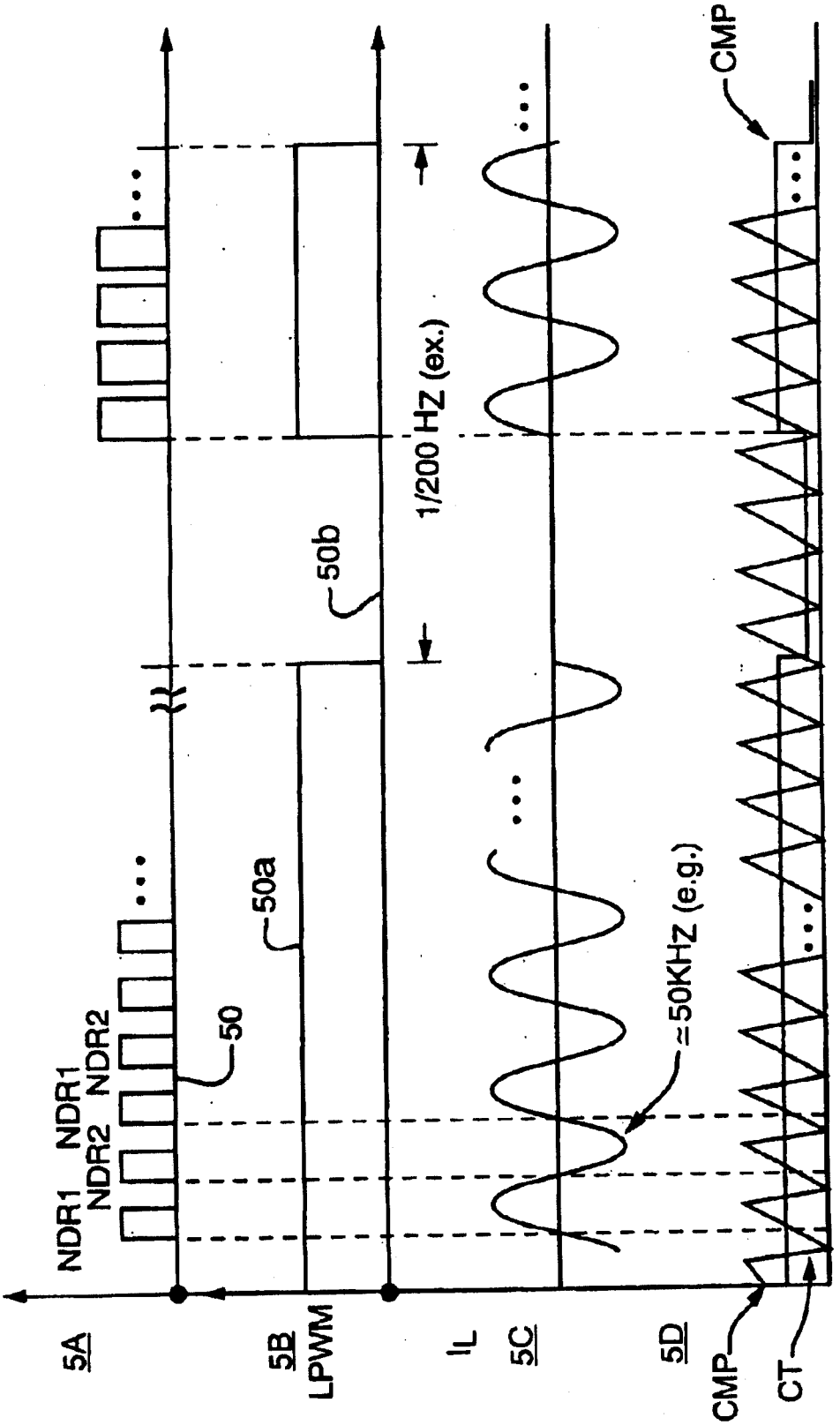

NDR1
NDR2
NDR1
NDR2
50
50a
50b
1/200 Hz (ex.)
≈50KHz (e.g.)
CMP
5A
5B
LPWM
IL
5C
5D
CMP
CT

FIG. 5

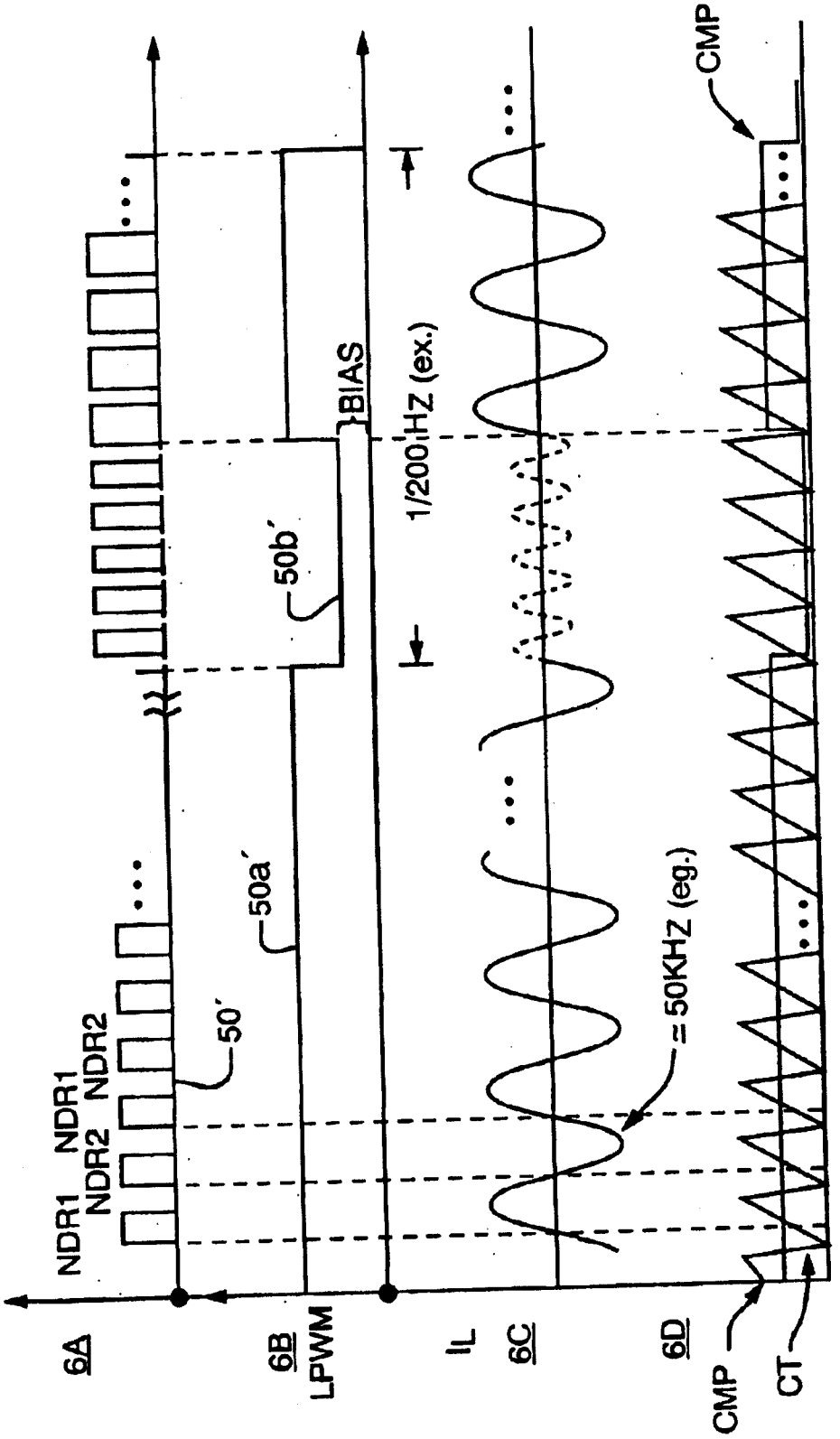

NDR1
NDR2
NDR1
NDR2
50'
50a'
50b'
BIAS
1/200 HZ (ex.)
= 50KHZ (eg.)
CMP
6A
6B
LPWM
IL
6C
6D
CMP
CT

FIG. 6

INVERTER CONTROLLER

FIELD OF THE INVENTION

The present invention relates to an inverter controller, and more particularly, to an inverter controller that utilizes pin multiplexing and/or pin multitasking techniques to reduce the overall pin count and reduce the number of components, without reducing the functionality and/or performance of the controller. Particular utility for the present invention is for a two-switch DC/AC inverter topology for driving a CCFL, however, other inverter topologies and/or DC/DC converter topologies, and/or other loads are equally contemplated herein.

SUMMARY OF THE INVENTION

The present invention provides an integrated circuit that includes an inverter controller being adapted to generate a plurality of signals to drive an inverter circuit. The controller also includes one or more input pins configured to receive two or more input signals. Each signal supports an associated function of the controller.

In one exemplary embodiment, the input pin is configured to receive a first signal representing a dim voltage, where the first signal has a first voltage range. The pin is also configured to receive a second signal representing a voltage feedback signal, where the second signal has a second voltage range.

In another exemplary embodiment, the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period. The pin is also configured to receive a second signal representing a soft start signal, where the second signal is present in a second time period.

The present invention also provides an inverter controller IC that includes a multiplexer circuit to direct one input signal to a first circuit to support a first function of the controller, and to direct another of the input signals to a second circuit to support a second said function of the controller.

The present invention further provides an inverter controller IC that includes an input pin configured to receive two or more input signals, each signal supports an associated function of the controller. One of the input signals is present in a first time period and another of the input signals is present in a second time period.

Thus, according to the present invention pin count may be significantly reduced. Also, by choosing which pins may be multifunctional and/or multiplexed, the present invention decreases tooling and PCB layout requirements.

Additional benefits and advantages of the present invention will become apparent to those skilled in the art to which this invention relates from the subsequent description of the preferred embodiments and the appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of one exemplary inverter controller integrated circuit according to the present invention;

FIG. **2** is a block diagram of another exemplary inverter controller integrated circuit according to the present invention;

FIG. **3** depicts an exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **4** depicts another exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **5** depicts representative signal graphs for certain signals generated by the controller of FIG. **1**; and

FIG. **6** depicts representative signal graphs for certain signals generated by the controller of FIG. **2**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** depicts a block diagram of an exemplary inverter controller integrated circuit **10** according to the present invention. In this exemplary embodiment, the controller **10** is an 8 pin design (labeled 1–8), where pin **2** is adapted to receive two signals and multiplexed to support two functions, and pin **4** is adapted to receive two signals to support two functions, depending on the state certain components of the controller. In this example, pin **2** supports both load voltage sensing and dim signal sensing. Pin **4** supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

The controller **10** includes an overvoltage protection circuit **100**, a dimming circuit **200**, a current feedback control circuit **300** and an output circuit **400**. The controller **10** also includes a MUX **18** to control switching of the function of PIN **2** between load voltage sensing and dimming signal input control, based on the state of the load. The controller also includes an oscillator circuit **12** that generates a sawtooth signal **14** by charging/discharging a fixed capacitor CT **16**, and a reference signal/bias signal generator **20** that generates one or more of the reference and/or bias signals utilized by the controller **10**. The controller operates to generate two switch driving signals NDR1 and NDR2. The drive control signals may be used to drive the two switches of a derived Royer circuit, a push pull circuit, a half bridge circuit or other two-switch inverter circuit known in the art.

Stated another way, the present invention provides an inverter controller that includes a one or more multiplexed and/or multifunctional pins, where the controller is adapted to generate one or more control signals based on the signal state of the multiplexed and/or multifunctional pins. The following description of the overvoltage protection circuit **100**, the dimming circuit **200**, the current control circuit **300** and the output circuit **400** will be readily understood by those skilled in the inverter arts. Each of the components of the controller **10** is described in greater detail below.

Output circuit **400** includes a comparator **42** that compares a signal **52** from the output of the error amplifier **30** with a sawtooth signal generated by the oscillator circuit **12**. The error signal **52** is generated by the current control circuit **300** and/or the CMP capacitor **40** (at PIN **4**), as also may be modified by the dimming circuit **200**. The error signal has a value to be within the range of the minimum and maximum value of the sawtooth signal **14** for normal operation. For example, for CCFL loads, the sawtooth signal may have a range between 0V and 3.0V. As is understood in the art, the intersection between the sawtooth signal **14** and the error signal **52** is used by the switch driver logic **44** to set the pulse width of each of the switch driver signals NDR1 and NDR2. Generally, the higher the error signal value, the wider the pulse width and thus, more power is delivered to the load (although the circuitry could be modified where the reverse is true).

As set forth above, the value of the error signal **52** is determined by current feedback information generated by

the current control circuit **300**, and modified by the dimming circuit **200**. As a general matter, The CMP capacitor **40** is charged during the initial power on of the controller **10**. Error amplifier **30** operates as a current source (e.g., transconductance amplifier) to adjust the charge on the CMP capacitor **40**. Amplifier **30** compares the load current Isens to a user-definable reference signal **32** indicative of maximum load current at maximum power or maximum brightness **32**. If the value of the load current is less than signal **32**, amplifier **30** will source current to charge the capacitor **40** in an attempt to increase the DC value of the error signal **52**, thereby increasing the pulse width of the output driver signals NDR1 and NDR2. If the value of the load current is greater than the reference signal **32**, amplifier **30** will sink charge from the CMP capacitor **40** to decrease the DC value of the error signal **52**, thereby decreasing the pulse width of the output driver signals NDR1 and NDR2. In other words, amplifier **30** represents a closed loop feedback current control that sources or sinks current to attempt to maintain the load current Isens approximately equal to the reference signal **32**.

Dimming circuitry **200** is enabled by the MUX circuit **18** (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN **2**). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry **200** is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal **50**) that its duty cycle is proportional to Vdim. The frequency of the burst mode signal **50** is selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35–80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

In the exemplary embodiment, dimming circuit **200** comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit **36** generates a burst mode signal **50** that has a duty cycle proprtial to the value of Vdim. In this example, the duty cycle of the burst mode signal **50** ranges from 0% (Vdim=V1) to 100% (Vdim=V2).

If the dimming circuit **200** is enabled by the MUX **18**, the PWM enable block **38** operates to sink charge from the CMP capacitor **40**. The enable block **38** may comprise a simple switch tied to ground whose conduction state is controlled by the burst mode signal **50**. As stated above, error amplifier **30** generates an output to maintain a DC signal **52** having a maximum value represented by signal **32**. The burst mode signal **50** operates as follows. When the burst mode signal is asserted (high or low), the enable circuit **38** sinks the charge from the capacitor **40**. The resulting DC signal **52** is a minimum value (e.g., 0 Volts). As a result, the signal generated by comparator **42** represents the intersection between the lowest value of the CT signal **14** and the DC signal **52**, and accordingly the switch driver logic **44** turns the driving signals NDR1 and NDR2 off while the burst mode signal is asserted. When the burst mode signal is deasserted, the PWM enable block essentially becomes an open circuit and the error amplifier **30** recharges capacitor **40** to the original value. The resulting error signal resumes to the value corresponding to the maximum brightness output as described above, and accordingly the switch logic driver generates driving signals NDR1 and NDR2 having a duty cycle corresponding to the maximum brightness output. Thus, burst mode operation, in this exemplary embodiment swings the output from fully on to fully off at a frequency determined by the burst mode signal **50**.

PIN **2** is adapted to receive two signals representing both load voltage sensing (Vsens) and DIM signal input. The DIM signal (Vdim) is used to support power control of the load. Load voltage control is used, for example, to detect an overvoltage condition at the load. In this example, a multiplexer MUX **18** is utilized to direct the input on PIN **2** (either Vsens or Vdim) into the overvoltage protection circuit **100** or the dimming circuit **200**, based on a predetermined condition. In this example, the predetermined condition is a lamp on signal **34** which indicates that a lamp load is present and working properly, where signal **34** is an input to the MUX **18**. In this exemplary embodiment, the DIM signal is fixed to a predetermined range, i.e., V1<Vdim<V2. Vsens is configured to be outside this range, i.e., Vsens>V2, or Vsens<V1.

When the controller is initially powered on to drive a load, the controller will receive both load voltage and load current feedback to determine if the load is operating properly. Current feedback is represented by Isens at PIN **3**, and voltage feedback is represented by Vsens at PIN **2**. Assuming a lamp load (e.g., CCFL), those skilled in the art will recognize that a broken or missing lamp can create a dangerously high voltage situation at the secondary side of a transformer (not shown in FIG. **1**). Thus, the present invention initially determines the status of the lamp load by checking if a minimum current is being delivered to the load.

To that end, comparator **28** compares the load current Isens with a lamp threshold signal **46**. The lamp threshold signal **46** is a signal indicative of the minimum current that should be present at the load if the load is working properly. If Isens is greater than or equal to signal **46**, comparator **28** generates a lamp on signal **34** indicative that the load is properly working. The lamp on signal **34** is a control signal generated by the comparator **28** that controls the state of the MUX **18**. In this case, the lamp on signal sets the output state of the MUX to couple the dimming circuitry **200** to PIN **2**. A latch circuit **74** is provided to latch the output of the lamp on signal once Isens exceeds the threshold signal **46**. The lamp on signal will remain in this state during normal operation, so that burst mode dimming (described below) does not change the state of the lamp on signal. The Vdim input on PIN2 is then used to set the desired dim brightness value (as will be described below).

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit **74** is set), the current sense value Isens stays below the lamp threshold signal **46**, the output of the amplifier **28** changes the state of the lamp on signal **34**. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit **100** to PIN **2**. As is understood in the CCFL arts, Vsens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however, and open or broken lamp condition exists, Vsens will rise to a value greater than V2. When PIN **2** is coupled to the overvoltage protection circuit **100**, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in comparator **22**. When Vsens exceeds Vovp **48**, the output of comparator causes timing circuit **24** to initiates a predefined timeout period.

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal **46**. Also, error amplifier **30** will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the timout period, the protection circuit operates in a manner similar to the PWM enable circuit **38**. During this period, to prevent the error amplifier from generating a error singal to cause the switches to drive at higher power, the OVP signal **60** stops the error amplifier **30** to charge/discharge of CMP capacitor **40** At the end of the timout, the protection circuit **26** disables the switch driver logic **44** and thus the output overvoltage is controlled.

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit **100** configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit **200** configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit **300** configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit **400** configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN **2**) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer **18** coupled to the pin and configured to direct the voltage feedback signal to the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

PIN **4** and the CMP capacitor also operates to control soft start (SST) functionality. Soft start, as is known in the art, essentially operates in the beginning of power on, to cause the output circuitry to generate a minimal pulse width and gradually increase the pulse width. At initial power on the voltage on the CMP capacitor is zero. Isens is also zero, and therefore the error amplifier attempts to source the CMP capacitor to a charge that satisfies signal **32**. The time this process takes is dependent on the desired charge on CMP and the capacitance of CMP, and therefore this time period is utilized as soft start. This ensures that the amount of power to the load is increased gradually. It continues until the load current value reaches the threshold value 32. Then the error amplifier **30** takes over the control of PIN **4** which is the charge on the capacitor, as described herein. For CCFL loads, it is known that a gradual increase in lamp current helps to ensure the life of the lamp.

Thus, PIN **4** is adapted to generate the DC signal CMP **52** based on the values of the error signal generated by the current control circuit **300** and/or the dimming signal generated by the dimming circuit **200**. PIN **4** is multifunctional since it is also adapted to generate a soft start signal **52** based on the value of the error signal generated by the current control circuit **300**.

FIG. **5** depicts representative signal graphs for certain signals generated by the controller **10** of the present invention. FIG. **5**A shows the drive signals NDR**1** and NDR**2**. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **5**D. FIG. **5**B depicts the burst mode signal (LPWM) **50**, and FIG. **5**C depicts the load current I_L. When the burst mode signal is deasserted (high) **50**A, the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50**B, the drive signals stop and the lamp current is approximately zero. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (approximately zero) as described above.

FIG. **2** depicts another exemplary inverter controller **10'** according to the present invention. The inverter controller **10'** of this exemplary embodiment operates in a similar manner as described above with reference to FIG. **1**, but includes additional circuitry which may be desirable for a given operating environment. For example, at the output of error amplifier **30** is an on/off circuit triggered by the OVP signal. If the overvoltage protection circuit is activated, the OVP signal shuts the output of the error amplifier **30** off, regardless of the value of Isens. Thus, when the OVP signal is asserted, block **30** neither sources nor sinks capacitor **40**. Of course, the protection circuitry may also be adapted to charge or discharge the capacitor **40** to some minimum level so that the output signals deliver a predetermined minimum pulse width to the load during the time out period.

The controller **10'** also includes a min/max circuit **56** which, during times when the burst mode signal is enabled, generates a minimum DC value (instead of a zero DC value 52, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the min/max circuit **56** generates an output to cause the output signals to have some predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintain continuous function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

An enable comparator **58** is provided to generate an enable control signal to the switch logic **44**. The comparator generates an enable signal (thereby enabling the switch logic) if the value on the capacitor **40** is greater than the enable threshold value or else the switch logic is disabled.

The PWM enable circuit **38'** may include a floor value (i.e., bias), below which the PWM enable circuit will not sink charge from the CMP capacitor **40**. Like the min/max circuit, this prevents the burst mode enabled signal from completely sinking the charge on the capacitor, so that the output signals are set at a predetermined minimum other than zero. The value of the bias may be selected in accordance with the operating range of the controller, a desired minimum power delivered to the load during burst mode assertion, and/or other factors that will be apparent to those skilled in the art.

FIG. **6** depicts representative signal graphs for certain signals generated by the controller **10'** of the present invention. FIG. **6**A shows the drive signals NDR**1** and NDR**2**. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **6**D. FIG. **6**B depicts the burst mode signal (LPWM) **50'**, and FIG. **6**C depicts the load current I_L. When the burst mode signal is deasserted (high) **50**A', the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50**B', the drive signals are reduced to a predetermined minimum pulse width and the lamp current is significantly reduced. The asserted value of the burst mode signal **50**B' is biased in a manner described above. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (greater than zero), as described above.

Thus, the exemplary inverter controller ICs **10** and **10'** of FIGS. **1** and **2** include a pin (e.g., PIN**2**) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverter controller ICs **10** and **10'** are

also adapted to include a pin (e.g., PIN **4**) that is multifunctional to operate is a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

FIG. **3** depicts an exemplary application topology for the inverter controller IC **10** or **10'**. The controller IC **10** or **10'** depicted in FIG. **3** is used to drive a derived Royer circuit comprised of transistors Q1 and Q2, to power a CCFL load **66**. Q1 and Q2 drive the primary side of the transformer **60**, through a resonant tank circuit formed by the capacitor **68** and the primary side inductance of the transformer **60**. The operation of this type of circuit is well known by those skilled in the art. Vsen is derived from a voltage divider between capacitors C1 and C2 (node **62**) so that the value of Vsen is nominal compared to the voltage at the secondary side of the transformer. Vsen is typically in the range of 1 to 5 Volts. Isen is derived from the CCFL load through the divider circuit of R1 and R2 (node **64**). Isen will typically range between 0 Volts (no lamp) to 1.25 Volts (full lamp brightness). Of course, these values are only exemplary, and may be modified to meet design criteria without departing from the present invention. FIG. **4** represents another exemplary application topology for the inverter controller **10** or **10'**. The controller in this embodiment is used to drive two (or more) CCFL loads **66** and **70**. In this case, since lamps **66** and **70** are in series, current feedback Isens is derived from the voltage divider **R1**, **R2**.

Those skilled in the art will recognize numerous modifications that may be made to the present invention. For example, the controller ICs **10** and **10'** of FIGS. **1** and **2** multiplex the values of Vsen and DIM on PIN **2**, and combine the functionality of the charge capacitor CMP **40** and soft start functionality. However, these are only examples of pin multiplexing/multitasking that may be accomplished by the present invention. Other pins associated with the exemplary IC may be multiplexed and/or multitasked. Additionally, other IC designs that require more or fewer pins than the 8 pin IC depicted in FIGS. **1** and **2** may likewise include pin multitasking and/or multiplexing as provided herein.

Still other modifications may be made. In the exemplary controller ICs of FIGS. **1** and **2**, PIN **2** is multiplexed to support both load voltage sensing and dim signal input. The range of dim signals (V1<Vdim<V2), as disclosed above, and the overvoltage protection threshold Vovp are selected such that Vovp>V2. However, this relationship is not required for the present invention to operate properly. Indeed Vovp may be selected within or below the range of Vdim, since the Vdim value is used by the overvoltage protection circuit **100**, independent of the dim value. Alternatively, the multiplexed and/or multifunctional pins disclosed herein may be adapted to support three or more signals, using multiplexing and or multifunctional techniques provided herein.

Still other modifications may be made. For example, the exemplary application topologies of FIGS. **3** and **4** depict the controller ICs **10** or **10'** driving a derived Royer circuit formed by Q1 and Q2. However, the controller **10** or **10'** may be likewise applied to a push-pull inverter, a half bridge inverter and/or other type of two switch inverter topology known in the art. Yet further, the controller IC **10** or **10'** may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC **10** or **10'** to drive a four switch inverter topology (e.g., full bridge inverter).

The present invention is not limited to a CCFL load. Indeed the controller **10** or **10'** of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller **10** or **10'** of the present invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the load type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in FIG. **4**, numerous other topologies may be used, for example as described in U.S. Pat. No. 6,104,146, and U.S. patent application Ser. Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are incorporated by reference in their entirety.

A detailed discussion of the operation of certain components of FIGS. **1** and **2** has been omitted. For example, the operation of the oscillator circuit **12** and the operation of the switch logic **44** have been omitted since it is assumed that one skilled in the art will readily recognize both the operation and implementation of these features. Also, the timing of the drive signals NDR1 and NDR2 is not described at length herein, since the operation of these signals will be apparent to those skilled in the art. The preceding detailed description of the block diagrams of FIGS. **1** and **2** is largely directed to the functionality of the components. The components of FIGS. **1** and **2** may be off-the-shelf or custom components to achieve the functionality stated herein, and those skilled in the art will readily recognize that many circuit implementations may be used to accomplish the functionality stated herein, and all such alternatives are deemed within the scope of the present invention.

Still further, inverter controller circuits that include voltage and current feedback, and dimming control (as described herein) are well known to those skilled in the art. However, the prior art integrated circuit inverter controllers have failed to address the long-felt need to reduce the IC package pin count while maintaining the functionality of the inverter IC. The present invention described herein provides examples of addressing this issue by providing, for example, multiplexed and/or multifunctional IC pins. Numerous modifications to this inventive theme will be apparent to those skilled in the art, and all such modifications are deemed within the scope of the present invention, as set forth in the claims.

What is claimed is:

1. A system, comprising:

one or more cold cathode fluorescent lamps;

an inverter circuit generating an AC signal to power said one or more lamps; and

an inverter controller adapted to generate a plurality of signals to drive said inverter circuit, said controller comprising at least one input pin configured to receive at least two independent input signals, each said input signal supporting an associated function of said controller during operation of said controller.

2. The system as claimed in claim **1**, wherein said inverter circuit is selected from a push-pull, half bridge and full-bridge inverter topologies for converting a DC signal to said AC signal.

3. The system as claimed in claim **1**, wherein said inverter circuit comprises a plurality of power switches for converting a DC signal to said AC signal.

4. The system as claimed in claim **1**, wherein said inverter circuit comprises a step-up transformer receiving said AC signal and generating a stepped-up AC signal.

5. The system as claimed in claim **1**, wherein said input pin configured to operate with a first signal representing a dim voltage, said first signal having a first voltage range; and a second signal representing a voltage feedback signal indicative of voltage supplied to said CCFL, said second signal having a second voltage range.

6. The system as claimed in claim 1, further comprising a multiplexer circuit to direct one of said input signals to a first circuit to support a first said function of said controller, and to direct another of said input signals to a second circuit to support a second said function of said controller.

7. The system as claimed in claim 1, wherein one of said input signals is present in a first time period and another of said input signals is present in a second time period.

* * * * *

EXHIBIT B

US006809938B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.: US 6,809,938 B2**
(45) **Date of Patent: Oct. 26, 2004**

(54) **INVERTER CONTROLLER**

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(73) Assignee: **O2Micro International Limited**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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Related U.S. Application Data

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(51) **Int. Cl.**[7] **H02M 3/335**
(52) **U.S. Cl.** **363/17**; 363/132; 315/307
(58) **Field of Search** 345/204, 205, 345/208, 210, 211, 212; 315/306, 307; 363/25, 17, 131, 132; 713/1; 323/905

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,615,093	A *	3/1997	Nalbant	363/25
6,198,236	B1 *	3/2001	O'Neill	315/307
6,640,271	B2 *	10/2003	Ehrenhardt et al.	710/100

* cited by examiner

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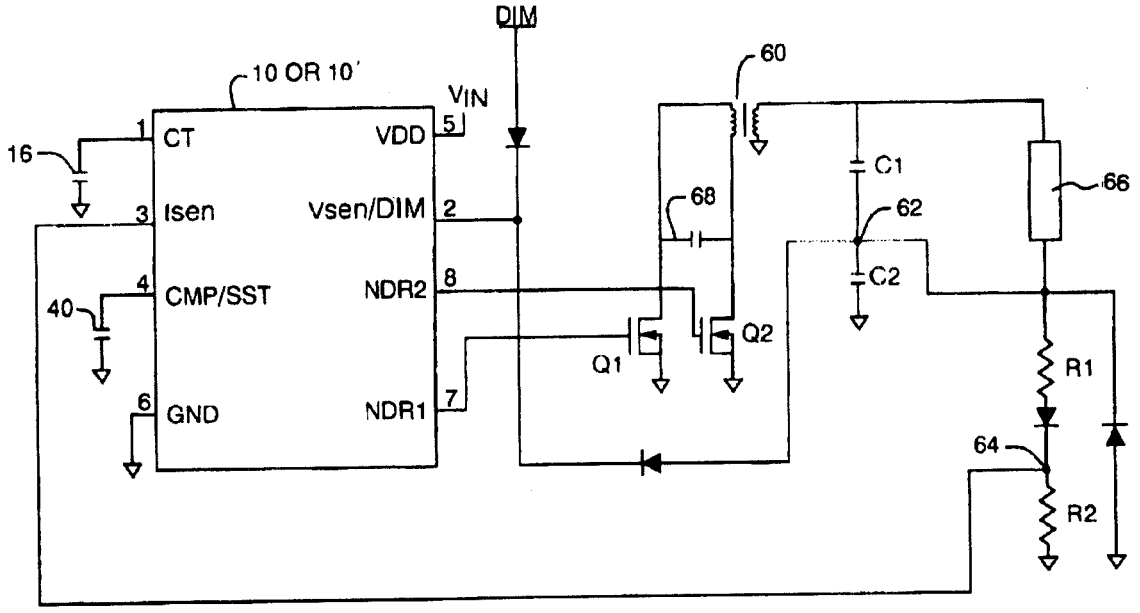
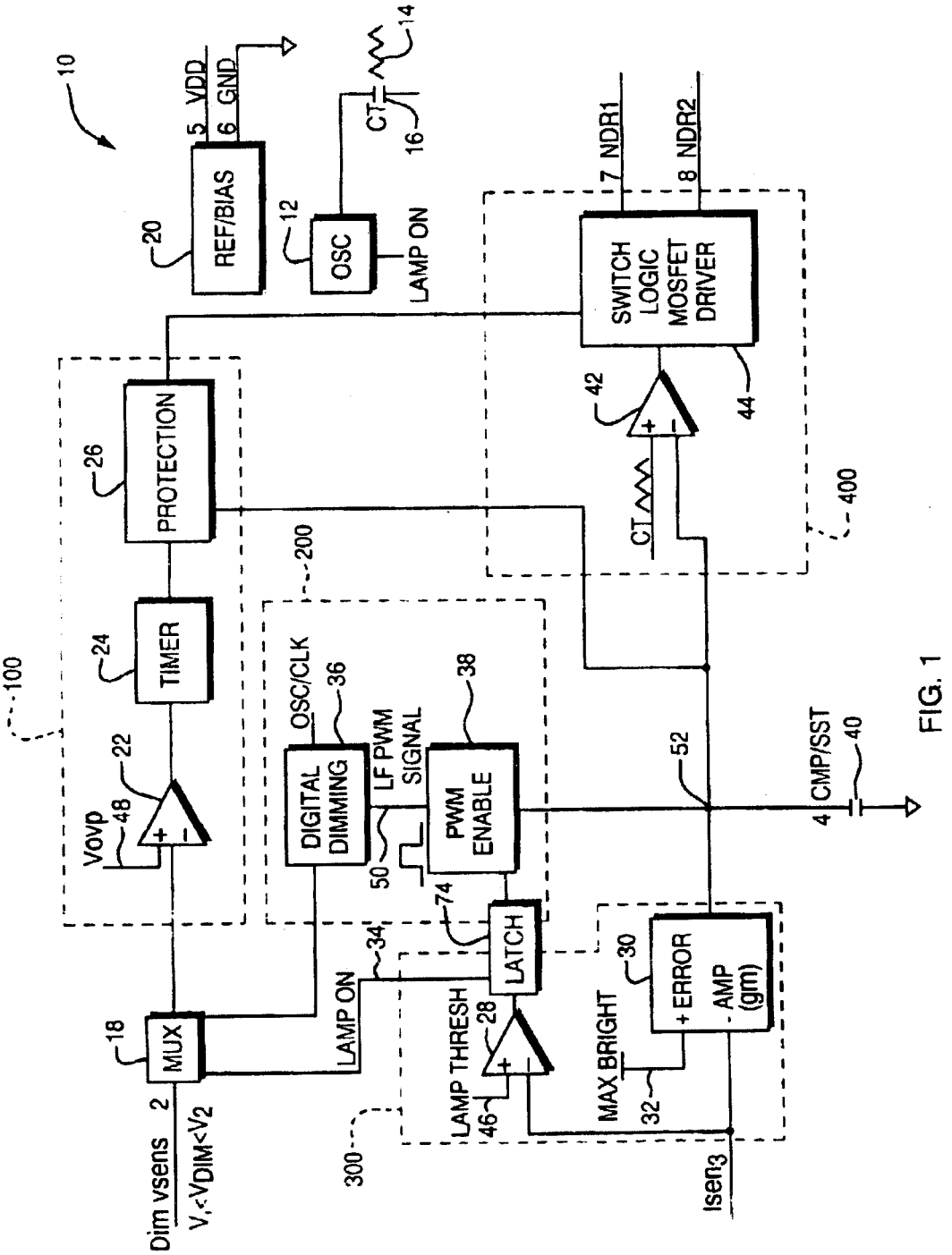
(57) **ABSTRACT**

An integrated circuit inverter controller that includes at least one input pin that is configured to receive two or more input signals. The input pin may be multiplexed so that the appropriate input signal is directed to appropriate circuitry within the controller to support two or more functions of the controller. Alternatively, the input signals may be present in differing time periods so that a single pin can support two or more functions. Multifunctional or multitasked pins reduce the overall pin count of the inverter controller.

6 Claims, 6 Drawing Sheets




10
5 VDD
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14
CT
16
REF/BIAS
20
12
OSC
LAMP ON
7 NDR1
8 NDR2
SWITCH LOGIC MOSFET DRIVER
42
44
PROTECTION
26
CT
400
200
TIMER
24
100
OSC/CLK
36
38
22
DIGITAL DIMMING
LF PWM SIGNAL
PWM ENABLE
52
CMP/SST
40
4
Vovp
48
50
74
LATCH
34
LAMP ON
30
+ ERROR AMP (gm) -
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MUX
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LAMP THRESH
MAX BRIGHT
32
46
2
300
Dim vsens
Isen3

FIG. 1

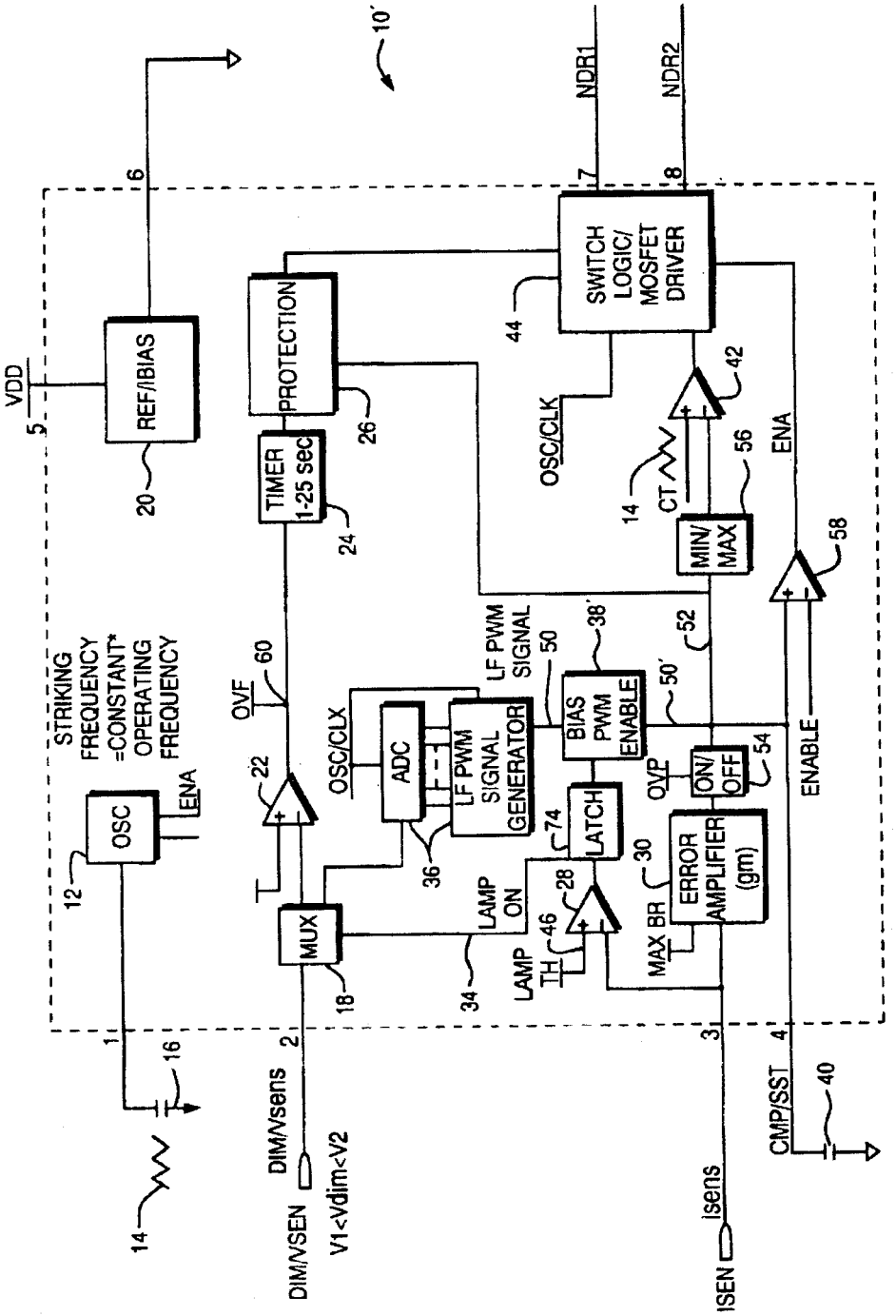
10'
NDR1
NDR2
VDD
REF/IBIAS
PROTECTION
TIMER 1-25 sec
SWITCH LOGIC/ MOSFET DRIVER
OSC/CLK
CT
MIN/ MAX
ENA
LF PWM SIGNAL
BIAS PWM ENABLE
OVF
OSC/CLX
ADC
LF PWM SIGNAL GENERATOR
OVP
ON/ OFF
LATCH
ERROR AMPLIFIER (gm)
MAX BR
LAMP ON
LAMP TH
MUX
OSC
STRIKING FREQUENCY =CONSTANT* OPERATING FREQUENCY
ENA
ENABLE
DIM/Vsens
V1<Vdim<V2
DIM/VSEN
Isens
ISEN
CMP/SST

FIG. 2

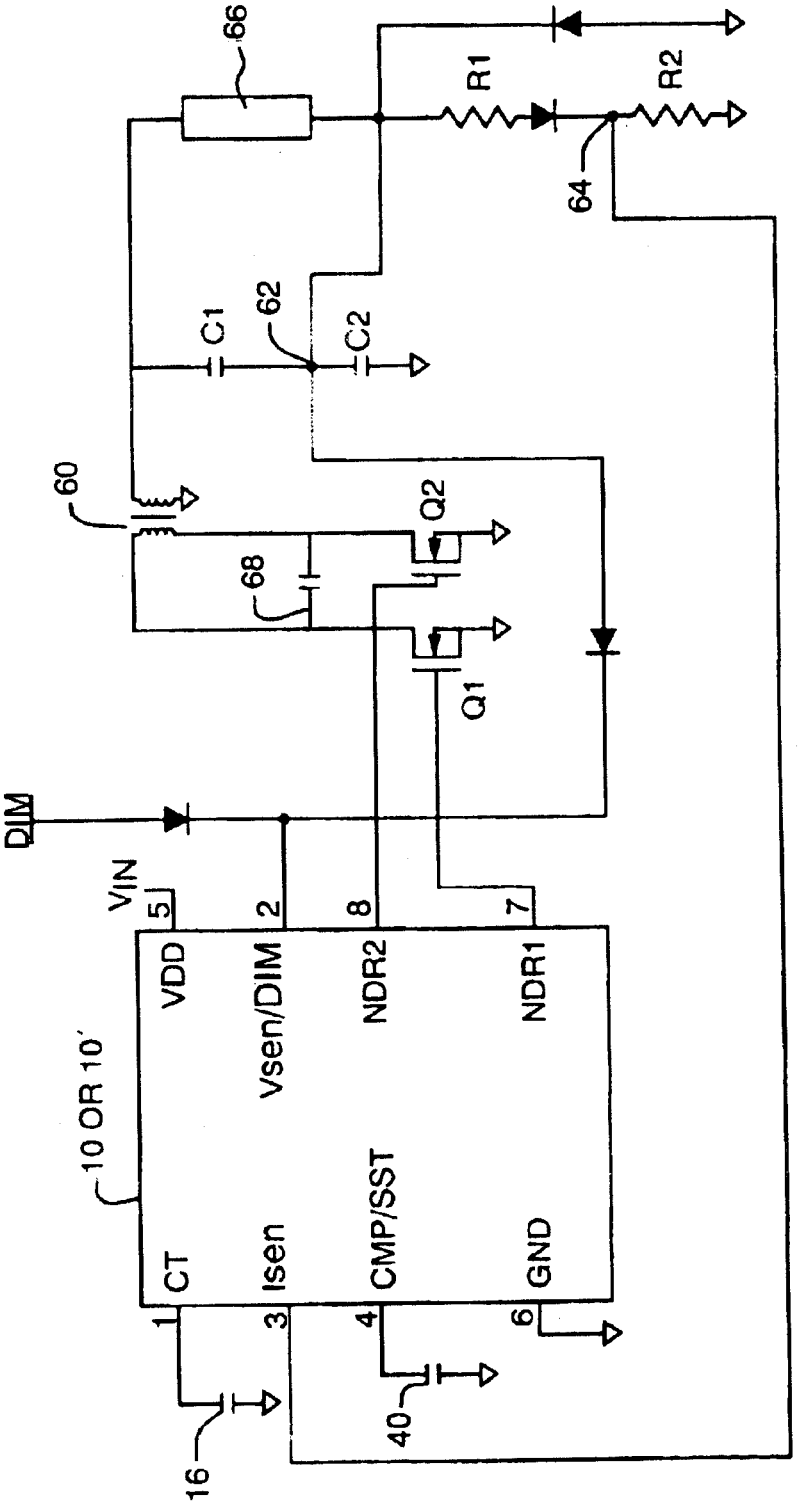
66
R1
R2
64
C1
62
C2
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen/DIM
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
40
16

FIG. 3

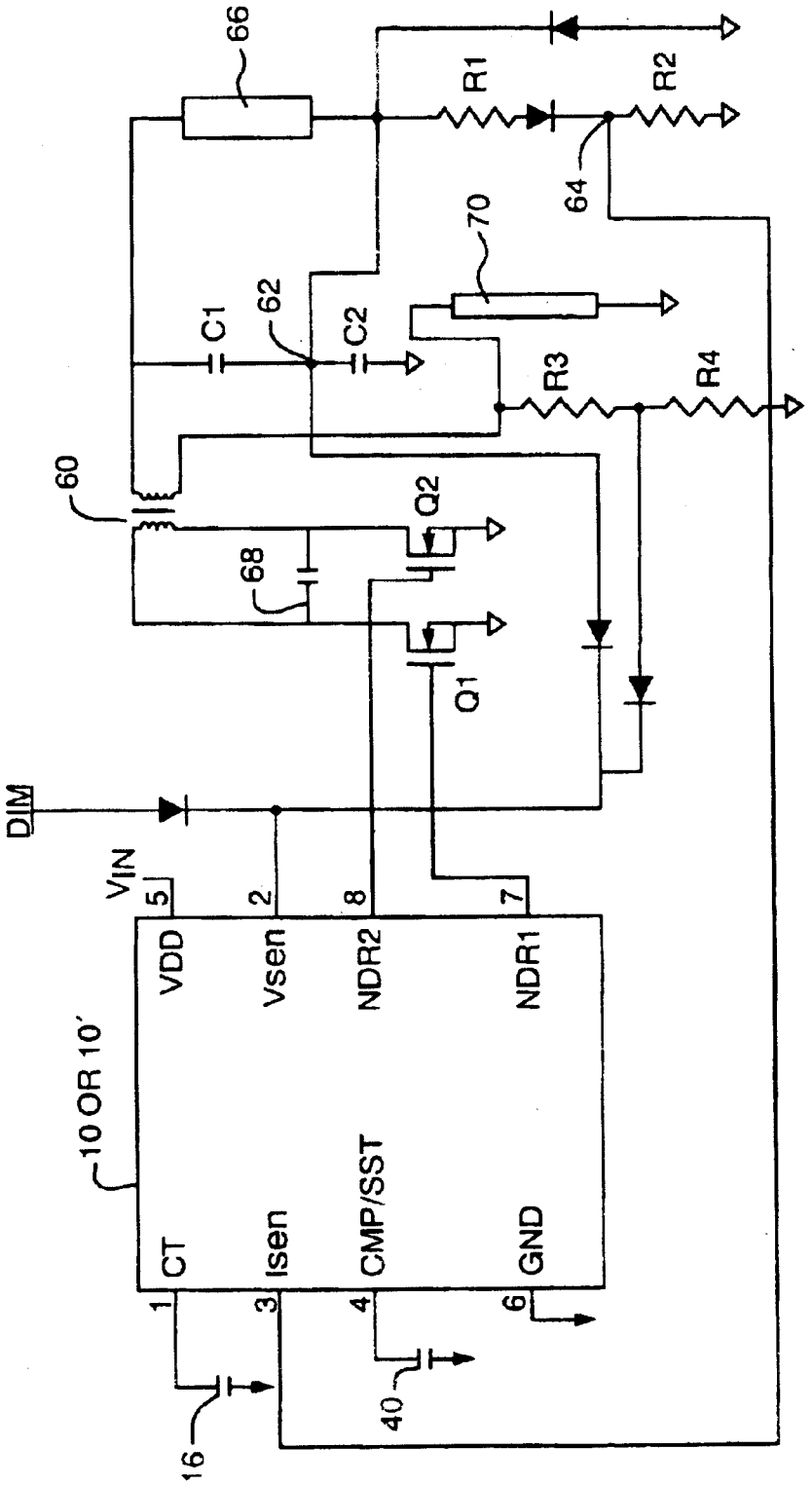
66
R1
R2
64
70
C1
62
C2
R3
R4
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
40
16

FIG. 4

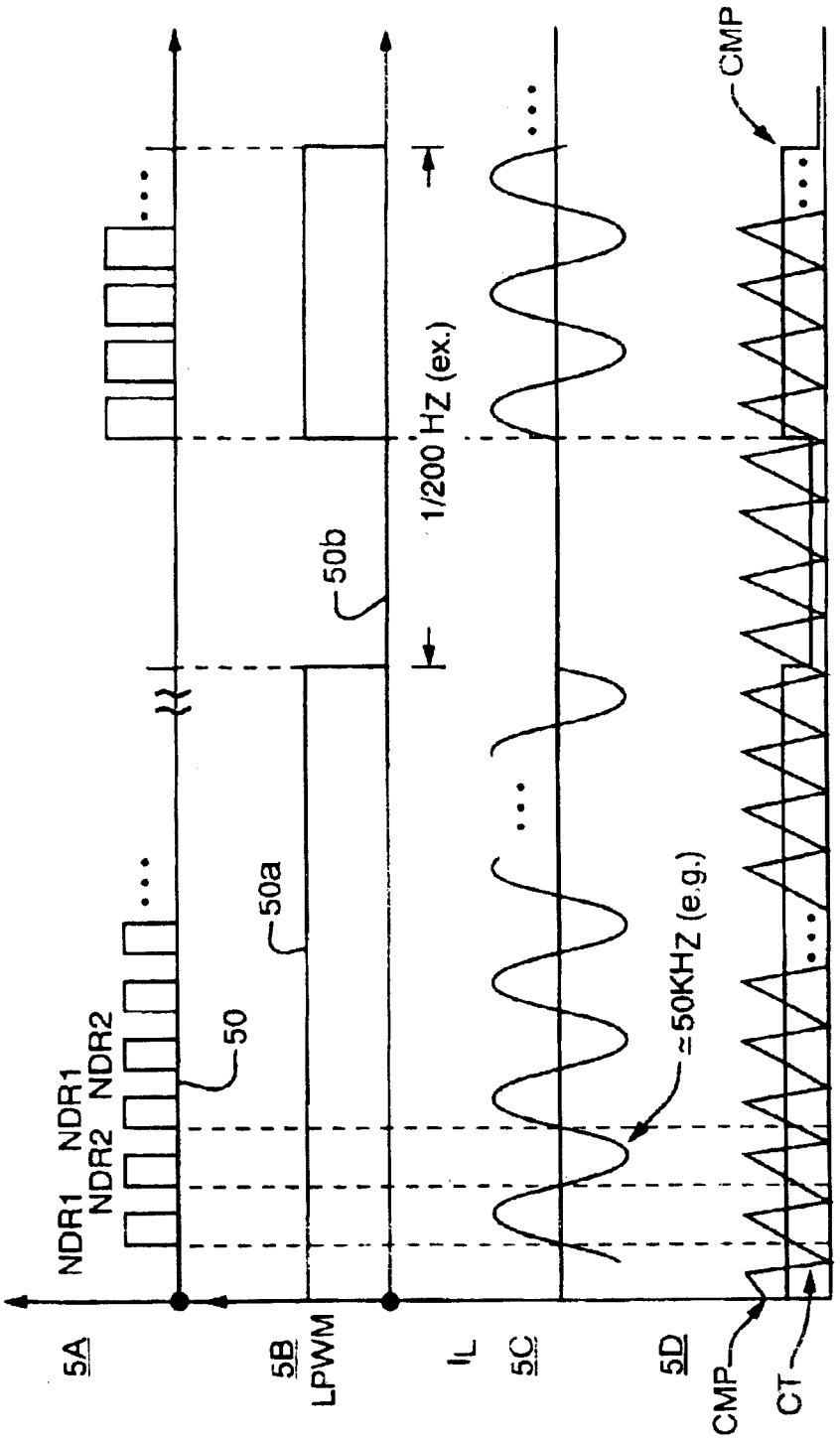
NDR1
NDR2
NDR1
NDR2
50
50a
50b
1/200 HZ (ex.)
≃50KHZ (e.g.)
CMP
5A
5B
LPWM
IL
5C
5D
CMP
CT

FIG. 5

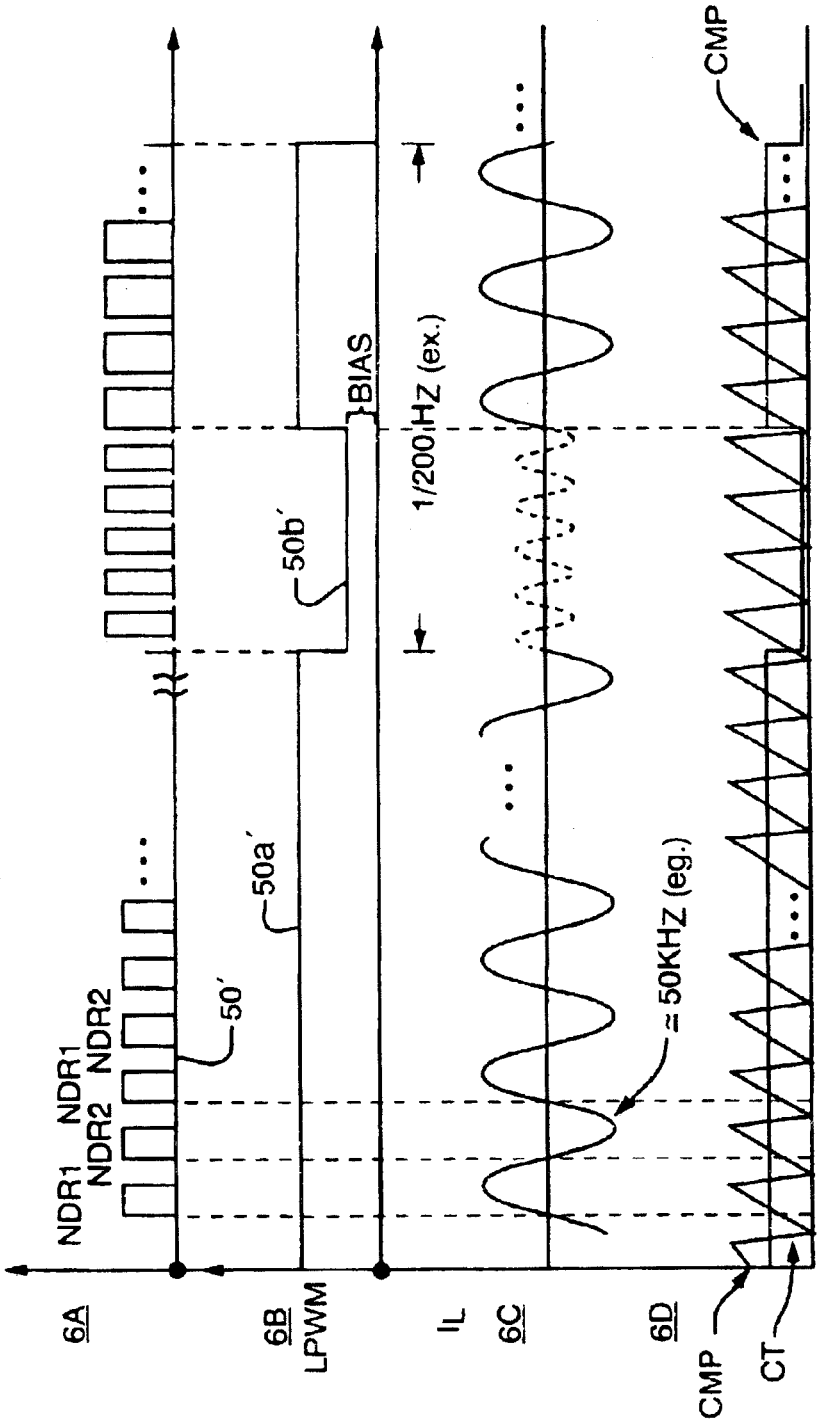
NDR1
NDR2
NDR1
NDR2
50'
50a'
50b'
BIAS
1/200 HZ (ex.)
≈ 50KHZ (eg.)
CMP
6A
6B
LPWM
IL
6C
6D
CMP
CT

FIG. 6

INVERTER CONTROLLER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 10/139,619, filed May 6, 2002

FIELD OF THE INVENTION

The present invention relates to an inverter controller, and more particularly, to an inverter controller that utilizes pin multiplexing and/or pin multitasking techniques to reduce the overall pin count and reduce the number of components, without reducing the functionality and/or performance of the controller. Particular utility for the present invention is for a two-switch DC/AC inverter topology for driving a CCFL, however, other inverter topologies and/or DC/DC converter topologies, and/or other loads are equally contemplated herein.

SUMMARY OF THE INVENTION

The present invention provides an integrated circuit that includes an inverter controller being adapted to generate a plurality of signals to drive an inverter circuit. The controller also includes one or more input pins configured to receive two or more input signals. Each signal supports an associated function of the controller.

In one exemplary embodiment, the input pin is configured to receive a first signal representing a dim voltage, where the first signal has a first voltage range. The pin is also configured to receive a second signal representing a voltage feedback signal, where the second signal has a second voltage range.

In another exemplary embodiment, the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period. The pin is also configured to receive a second signal representing a soft start signal, where the second signal is present in a second time period.

The present invention also provides an inverter controller IC that includes a multiplexer circuit to direct one input signal to a first circuit to support a first function of the controller, and to direct another of the input signals to a second circuit to support a second said function of the controller.

The present invention further provides an inverter controller IC that includes an input pin configured to receive two or more input signals, each signal supports an associated function of the controller. One of the input signals is present in a first time period and another of the input signals is present in a second time period.

Thus, according to the present invention pin count may be significantly reduced. Also, by choosing which pins may be multifunctional and/or multiplexed, the present invention decreases tooling and PCB layout requirements.

Additional benefits and advantages of the present invention will become apparent to those skilled in the art to which this invention relates from the subsequent description of the preferred embodiments and the appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of one exemplary inverter controller integrated circuit according to the present invention;

FIG. **2** is a block diagram of another exemplary inverter controller integrated circuit according to the present invention;

FIG. **3** depicts an exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **4** depicts another exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **5** depicts representative signal graphs for certain signals generated by the controller of FIG. **1**; and

FIG. **6** depicts representative signal graphs for certain signals generated by the controller of FIG. **2**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** depicts a block diagram of an exemplary inverter controller integrated circuit **10** according to the present invention. In this exemplary embodiment, the controller **10** is an 8 pin design (labeled 1–8), where pin **2** is adapted to receive two signals and multiplexed to support two functions, and pin **4** is adapted to receive two signals to support two functions, depending on the state certain components of the controller. In this example, pin **2** supports both load voltage sensing and dim signal sensing. Pin **4** supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

The controller **10** includes an overvoltage protection circuit **100**, a dimming circuit **200**, a current feedback control circuit **300** and an output circuit **400**. The controller **10** also includes a MUX **18** to control switching of the function of PIN **2** between load voltage sensing and dimming signal input control, based on the state of the load. The controller also includes an oscillator circuit **12** that generates a sawtooth signal **14** by charging/discharging a fixed capacitor CT **16**, and a reference signal/bias signal generator **20** that generates one or more of the reference and/or bias signals utilized by the controller **10**. The controller operates to generate two switch driving signals NDR1 and NDR2. The drive control signals may be used to drive the two switches of a derived Royer circuit, a push pull circuit, a half bridge circuit or other two-switch inverter circuit known in the art.

Stated another way, the present invention provides an inverter controller that includes a one or more multiplexed and/or multifunctional pins, where the controller is adapted to generate one or more control signals based on the signal state of the multiplexed and/or multifunctional pins. The following description of the overvoltage protection circuit **100**, the dimming circuit **200**, the current control circuit **300** and the output circuit **400** will be readily understood by those skilled in the inverter arts. Each of the components of the controller **10** is described in greater detail below.

Output circuit **400** includes a comparator **42** that compares a signal **52** from the output of the error amplifier **30** with a sawtooth signal generated by the oscillator circuit **12**. The error signal **52** is generated by the current control circuit **300** and/or the CMP capacitor **40** (at PIN **4**), as also may be modified by the dimming circuit **200**. The error signal has a value to be within the range of the minimum and maximum value of the sawtooth signal **14** for normal operation. For example, for CCFL loads, the sawtooth signal may have a range between 0V and 3.0V. As is understood in the art, the intersection between the sawtooth signal **14** and the error signal **52** is used by the switch driver logic **44** to set the pulse width of each of the switch driver signals NDR1 and NDR2. Generally, the higher the error signal value, the wider the

pulse width and thus, more power is delivered to the load (although the circuitry could be modified where the reverse is true).

As set forth above, the value of the error signal **52** is determined by current feedback information generated by the current control circuit **300**, and modified by the dimming circuit **200**. As a general matter, The CMP capacitor **40** is charged during the initial power on of the controller **10**. Error amplifier **30** operates as a current source (e.g., transconductance amplifier) to adjust the charge on the CMP capacitor **40**. Amplifier **30** compares the load current Isens to a user-definable reference signal **32** indicative of maximum load current at maximum power or maximum brightness **32**. If the value of the load current is less than signal **32**, amplifier **30** will source current to charge the capacitor **40** in an attempt to increase the DC value of the error signal **52**, thereby increasing the pulse width of the output driver signals NDR1 and NDR2. If the value of the load current is greater than the reference signal **32**, amplifier **30** will sink charge from the CMP capacitor **40** to decrease the DC value of the error signal **52**, thereby decreasing the pulse width of the output driver signals NDR1 and NDR2. In other words, amplifier **30** represents a closed loop feedback current control that sources or sinks current to attempt to maintain the load current Isens approximately equal to the reference signal **32**.

Dimming circuitry **200** is enabled by the MUX circuit **18** (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN **2**). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry **200** is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal **50**) that its duty cycle is proportional to Vdim. The frequency of the burst mode signal **50** is selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35–80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

In the exemplary embodiment; dimming circuit **200** comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit **36** generates a burst mode signal **50** that has a duty cycle proprtial to the value of Vdim. In this example, the duty cycle of the burst mode signal **50** ranges from 0% (Vdim=V1) to 100% (Vdim=V2).

If the dimming circuit **200** is enabled by the MUX **18**, the PWM enable block **38** operates to sink charge from the CMP capacitor **40**. The enable block **38** may comprise a simple switch tied to ground whose conduction state is controlled by the burst mode signal **50**. As stated above, error amplifier **30** generates an output to maintain a DC signal **52** having a maximum value represented by signal **32**. The burst mode signal **50** operates as follows. When the burst mode, signal is asserted (high or low), the enable circuit **38** sinks the charge from the capacitor **40**. The resulting DC signal **52** is a minimum value ,(e.g., 0 Volts). As a result, the signal generated by comparator **42** represents the intersection between the lowest value of the CT signal **14** and the DC signal **52**, and accordingly the switch driver logic **44** turns the driving signals NDR1 and NDR2 off while the burst mode signal is asserted. When the burst mode signal is deasserted, the PWM enable block essentially becomes an open circuit and the error amplifier **30** recharges capacitor **40** to the original value. The resulting error signal resumes to the value corresponding to the maximum brightness output as described above, and accordingly the switch logic driver generates driving signals NDR1 and NDR2 having a duty cycle corresponding to the maximum brightness output. Thus, burst mode operation, in this exemplary embodiment swings the output from fully on to fully off at a frequency determined by the burst mode signal **50**.

PIN **2** is adapted to receive two signals representing both load voltage sensing (Vsens) and DIM signal input. The DIM signal (Vdim) is used to support power control of the load. Load voltage control is used, for example, to detect an overvoltage condition at the load. In this example, a multiplexer MUX **18** is utilized to direct the input on PIN **2** (either Vsens or Vdim) into the overvoltage protection circuit **100** or the dimming circuit **200**, based on a predetermined condition. In this example, the predetermined condition is a lamp on signal **34** which indicates that a lamp load is present and working properly, where signal **34** is an input to the MUX **18**. In this exemplary embodiment, the DIM signal is fixed to a predetermined range, i.e., V1<Vdim<V2. Vsens is configured to be outside this range, i.e., Vsens>V2, or Vsens<V1.

When the controller is initially powered on to drive a load, the controller will receive both load voltage and load current feedback to determine if the load is operating properly. Current feedback is represented by Isens at PIN **3**, and voltage feedback is represented by Vsens at PIN **2**. Assuming a lamp load (e.g., CCFL), those skilled in the art will recognize that a broken or missing lamp can create a dangerously high voltage situation at the secondary side of a transformer (not shown in FIG. **1**). Thus, the present invention initially determines the status of the lamp load by checking if a minimum current is being delivered to the load.

To that end, comparator **28** compares the load current Isens with a lamp threshold signal **46**. The lamp threshold signal **46** is a signal indicative of the minimum current that should be present at the load if the load is working properly. If Isens is greater than or equal to signal **46**, comparator **28** generates a lamp on signal **34** indicative that the load is properly working. The lamp on signal **34** is a control signal generated by the comparator **28** that controls the state of the MUX **18**. In this case, the lamp on signal sets the output state of the MUX to couple the dimming circuitry **200** to PIN **2**. A latch circuit **74** is provided to latch the output of the lamp on signal once Isens exceeds the threshold signal **46**. The lamp on signal will remain in this state during normal operation, so that burst mode dimming (described below) does not change the state of the lamp on signal. The Vdim input on PIN **2** is then used to set the desired dim brightness value (as will be described below).

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit **74** is set), the current sense value Isens stays below the lamp threshold signal **46**, the output of the amplifier **28** changes the state of the lamp on signal **34**. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit **100** to PIN **2**. As is understood in the CCFL arts, Vsens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however and open or broken lamp condition exists, Vsens will rise to a value greater than V2. When PIN **2** is coupled to the overvoltage protection circuit

100, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in comparator 22. When Vsens exceeds Vovp 48, the output of comparator causes timing circuit 24 to initiates a predefined timeout period.

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal 46. Also, error amplifier 30 will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the timout period, the protection circuit operates in a manner similar to the PWM enable circuit 38. During this period, to prevent the error amplifier from generating a error singal to cause the switches to drive at higher power, the OVP signal 60 stops the error amplifier 30 to charge/discharge of CMP capacitor 40. At the end of the timout, the protection circuit 26 disables the switch driver logic 44 and thus the output overvoltage is controlled.

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit 100 configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit 200 configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit 300 configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit 400 configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN 2) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer 18 coupled to the pin and configured to direct the voltage feedback signal to the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

PIN 4 and the CMP capacitor also operates to control soft start (SST) functionality. Soft start, as is known in the art, essentially operates in the beginning of power on, to cause the output circuitry to generate a minimal pulse width and gradually increase the pulse width. At initial power on the voltage on the CMP capacitor is zero. Isens is also zero, and therefore the error amplifier attempts to source the CMP capacitor to a charge that satisfies signal 32. The time this process takes is dependent on the desired charge on CMP and the capacitance of CMP, and therefore this time period is utilized as soft start. This ensures that the amount of power to the load is increased gradually. It continues until the load current value reaches the threshold value 32. Then the error amplifier 30 takes over the control of PIN 4 which is the charge on the capacitor, as described herein. For CCFL loads, it is known that a gradual increase in lamp current helps to ensure the life of the lamp.

Thus, PIN 4 is adapted to generate the DC signal CMP 52 based on the values of the error signal generated by the current control circuit 300 and/or the dimming signal generated by the dimming circuit 200. PIN 4 is multifunctional since it is also adapted to generate a soft start signal 52 based on the value of the error signal generated by the current control circuit 300.

FIG. 5 depicts representative signal graphs for certain signals generated by the controller 10 of the present invention. FIG. 5A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP 52 and the sawtooth signal CT, as depicted in FIG. 5D. FIG. 5B depicts the burst mode signal (LPWM) 50, and FIG. 5C depicts the load current I_L. When the burst mode signal is deasserted (high) 50A, the drive signals and lamp current are present. When the burst mode signal is asserted (low) 50B, the drive signals stop and the lamp current is approximately zero. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (approximately zero) as described above.

FIG. 2 depicts another exemplary inverter controller 10' according to the present invention. The inverter controller 10' of this exemplary embodiment operates in a similar manner as described above with reference to FIG. 1, but includes additional circuitry which may be desirable for a given operating environment. For example, at the output of error amplifier 30 is an on/off circuit triggered by the OVP signal. If the overvoltage protection circuit is activated, the OVP signal shuts the output of the error amplifier 30 off, regardless of the value of Isens. Thus, when the OVP signal is asserted, block 30 neither sources nor sinks capacitor 40. Of course, the protection circuitry may also be adapted to charge or discharge the capacitor 40 to some minimum level so that the output signals deliver a predetermined minimum pulse width to the load during the time out period.

The controller 10' also includes a min/max circuit 56 which, during times when the burst mode signal is enabled, generates a minimum DC value (instead of a zero DC value 52, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the min/max, circuit 56 generates an output to cause the output signals to have some predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintain continuous function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

An enable comparator 58 is provided to generate an enable control signal to the switch logic 44. The comparator generates an enable signal (thereby enabling the switch logic) if the value on the capacitor 40 is greater than the enable threshold value or else the switch logic is disabled.

The PWM enable circuit 38' may include a floor value (i.e., bias), below which the PWM enable circuit will not sink charge from the CMP capacitor 40. Like the min/max circuit, this prevents the burst mode enabled signal from completely sinking the charge on the capacitor, so that the output signals are set at a predetermined minimum other than zero. The value of the bias may be selected in accordance with the operating range of the controller, a desired minimum power delivered to the load during burst mode assertion, and/or other factors that will be apparent to those skilled in the art.

FIG. 6 depicts representative signal graphs for certain signals generated by the controller 10' of the present invention. FIG. 6A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP 52 and the sawtooth signal CT, as depicted in FIG. 6D. FIG. 6B depicts the burst mode signal (LPWM) 50', and FIG. 6C depicts the load current I_L. When the burst mode signal is deasserted (high) 50A', the drive signals and lamp current are present. When the burst mode signal is asserted (low) 50B', the drive signals are reduced to a predetermined minimum pulse width and the lamp current is significantly reduced. The asserted value of the burst mode signal 50B' is biased in a manner described above. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (greater than zero), as described above.

Thus, the exemplary inverter controller ICs **10** and **10'** of FIGS. **1** and **2** include a pin (e.g., PIN **2**) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverter controller ICs **10** and **10'** are also adapted to include a pin (e.g., PIN **4**) that is multifunctional to operate is a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

FIG. **3** depicts an exemplary application topology for the inverter controller IC **10** or **10'**. The controller IC **10** or **10'** depicted in FIG. **3** is used to drive a derived Royer circuit comprised of transistors Q1 and Q2, to power a CCFL load **66**. Q1 and Q2 drive the primary side of the transformer **60**, through a resonant tank circuit formed by the capacitor **68** and the primary side inductance of the transformer **60**. The operation of this type of circuit is well known by those skilled in the art. Vsen is derived from a voltage divider between capacitors C1 and C2 (node **62**) so that the value of Vsen is nominal compared to the voltage at the secondary side of the transformer. Vsen is. typically in the range of 1 to 5 Volts. Isen is derived from the CCFL load through the divider circuit of R1 and R2 (node **64**). Isen will typically range between **0** Volts (no lamp) to 1.25 Volts (full lamp brightness). Of course, these values are only exemplary, and may be modified to meet design criteria without departing from the present invention. FIG. **4** represents another exemplary application topology for the inverter controller **10** or **10'**. The controller in this embodiment is used to drive two (or more) CCFL loads **66** and **70**. In this case, since lamps **66** and **70** are in series, current feedback Isens is derived from the voltage divider R1, R2.

Those skilled in the art will recognize numerous modifications that may be made to the present invention. For example, the controller ICs **10** and **10'** of FIGS. **1** and **2** multiplex the values of Vsen and DIM on PIN **2**, and combine the functionality of the charge capacitor CMP **40** and soft start functionality. However, these are only examples of pin multiplexing/multitasking that may be accomplished by the present invention. Other pins associated with the exemplary IC may be multiplexed and/or multitasked. Additionally, other IC designs that require more or fewer pins than the 8 pin IC depicted in FIGS. **1** and **2** may likewise include pin multitasking and/or multiplexing as provided herein.

Still other modifications may be made. In the exemplary controller ICs of FIGS. **1** and **2**, PIN **2** is multiplexed to support both load voltage sensing and dim signal input. The range of dim signals (V1<Vdim<V2), as disclosed above, and the overvoltage protection threshold Vovp are selected such that Vovp>V2. However, this relationship is not required for the present invention to operate properly. Indeed Vovp may be selected within or below the range of Vdim, since the Vdim value is used by the overvoltage protection circuit **100**, independent of the dim value. Alternatively, the multiplexed and/or multifunctional pins disclosed herein may be adapted to support three or more signals, using multiplexing and or multifunctional techniques provided herein.

Still other modifications may be made. For example, the exemplary application topologies of FIGS. **3** and **4** depict the controller ICs **10** or **10'** driving a derived Royer circuit formed by Q1 and Q2. However, the controller **10** or **10'** may be likewise applied to a push-pull inverter, a half bridge inverter and/or other type of two switch inverter topology known in the art. Yet further, the controller IC **10** or **10'** may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC **10** or **10'** to drive a four switch inverter topology (e.g., full bridge inverter).

The present invention is not limited to a CCFL load. Indeed the controller **10** or **10'** of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller **10** or **10'** of the present invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the load type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in FIG. **4**, numerous other topologies may be used, for example as described in U.S. Pat. No. 6,104,146, and U.S. patent application Ser. Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are incorporated by reference in their entirety.

A detailed discussion of the operation of certain components of FIGS. **1** and **2** has been omitted. For example, the operation of the oscillator circuit **12** and the operation of the switch logic **44** have been omitted since it is assumed that one skilled in the art will readily recognize both the operation and implementation of these features. Also, the timing of the drive signals NDR1 and NDR2 is not described at length herein, since the operation of these signals will be apparent to those skilled in the art. The preceding detailed description of the block diagrams of FIGS. **1** and **2** is largely directed to the functionality of the components. The components of FIGS. **1** and **2** may be off-the-shelf or custom components to achieve the functionality stated herein, and those skilled in the art will readily recognize that many circuit implementations may be used to accomplish the functionality stated herein, and all such alternatives are deemed within the scope of the present invention.

Still further, inverter controller circuits that include voltage and current feedback, and dimming control (as described herein) are well known to those skilled in the art. However, the prior art integrated circuit inverter controllers have failed to address the long-felt need to reduce the IC package pin count while maintaining the functionality of the inverter IC. The present invention described herein provides examples of addressing this issue by providing, for example, multiplexed and/or multifunctional IC pins. Numerous modifications to this inventive theme will be apparent to those skilled in the art, and all such modifications are deemed within the scope of the present invention, as set forth in the claims.

What is claimed is:

1. A DC/AC inverter, comprising:

a plurality of power switches for converting a DC signal to an AC signal;

a step-up transformer receiving said AC signal and generating a stepped-up AC signal; and

an inverter controller adapted to generate a plurality of signals to drive said plurality of power switches, said controller comprising at least one input pin configured to receive at least two independent input signals, each said input signal supporting an associated function of said controller during operation of said controller.

2. A DC/AC inverter as claimed in claim **1**, further comprising one or more cold cathode fluorescent lamps (CCFL), said lamps receiving said stepped-up AC signal.

3. A DC/AC inverter as claimed in claim **1**, wherein said power switches arranged to form an inverter circuit selected from a push-pull, half bridge and full-bridge inverter topologies.

4. A DC/AC inverter as claimed in claim 1, wherein said input pin configured to receive a first signal representing a dim voltage, said first signal having a first voltage range; and a second signal representing a voltage feedback signal indicative of voltage supplied to a load, said second signal having a second voltage range.

5. A DC/AC inverter as claimed in claim 1, further comprising a multiplexer circuit to direct one of said input signals to a first circuit to support a first said function of said controller, and to direct another of said input signals to a second circuit to support a second said function of said controller.

6. A DC/AC inverter as claimed in claim 1, wherein one of said input signals is present in a first time period and another of said input signals is present in a second time period.

* * * * *

EXHIBIT C

US006900993B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.: US 6,900,993 B2**
(45) **Date of Patent: *May 31, 2005**

(54) **INVERTER CONTROLLER**

(75) Inventors: **Yung-Lin Lin**, Palo Alto, CA (US); **Da Liu**, San Jose, CA (US)

(73) Assignee: **O2Micro International Limited**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/690,104**

(22) Filed: **Oct. 21, 2003**

(65) **Prior Publication Data**

US 2004/0085792 A1 May 6, 2004

Related U.S. Application Data

(62) Division of application No. 10/139,619, filed on May 6, 2002, now Pat. No. 6,856,519.

(51) **Int. Cl.**[7] **H02M 3/335**

(52) **U.S. Cl.** **363/17**; 363/132; 315/307; 323/905

(58) **Field of Search** 345/204, 205, 345/208, 210, 211, 212; 315/306, 307; 713/1; 363/17, 131, 132, 25; 323/905

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,198,236 B1 * 3/2001 O'Neill 315/307
6,640,271 B2 * 10/2003 Ehrenhardt et al. 713/1

* cited by examiner

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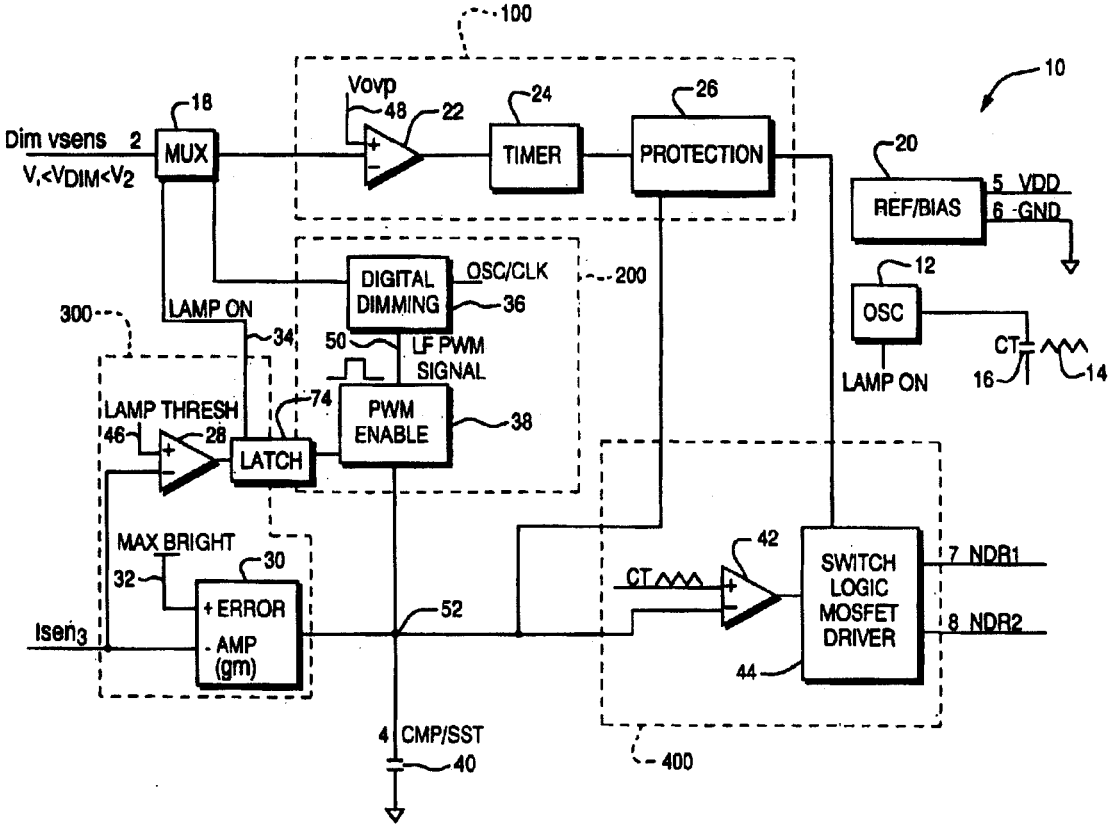
(57) **ABSTRACT**

An integrated circuit inverter controller that includes at least one input pin that is configured to receive two or more input signals. The input pin may be multiplexed so that the appropriate input signal is directed to appropriate circuitry within the controller to support two or more functions of the controller. Alternatively, the input signals may be present in differing time periods so that a single pin can support two or more functions. Multifunctional or multitasked pins reduce the overall pin count of the inverter controller.

7 Claims, 6 Drawing Sheets



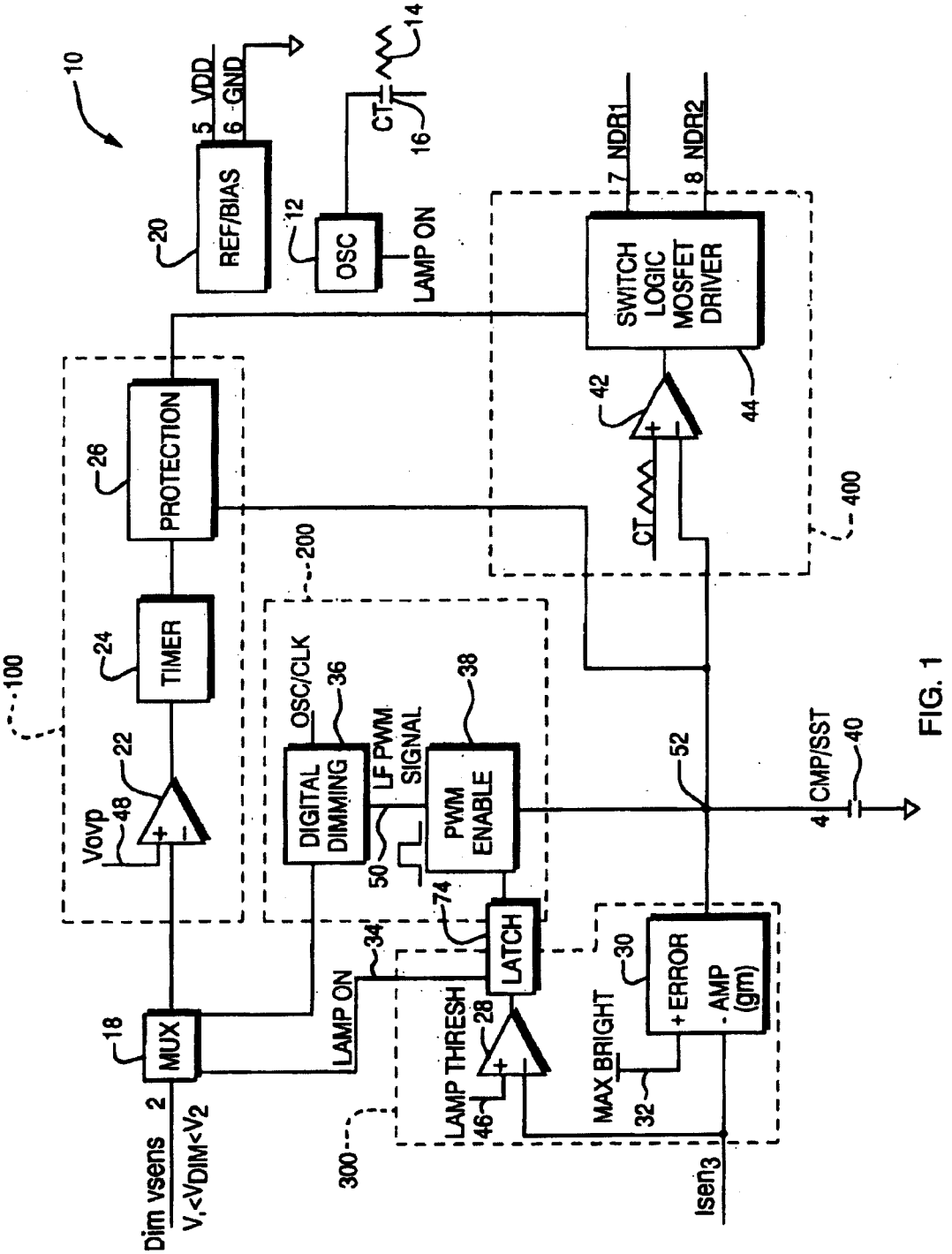

10
5 VDD
6 GND
14
CT
16
REF/BIAS
20
OSC
12
LAMP ON
7 NDR1
8 NDR2
SWITCH LOGIC MOSFET DRIVER
42
44
PROTECTION
26
CT
400
200
TIMER
24
100
OSC/CLK
36
DIGITAL DIMMING
LF PWM SIGNAL
38
PWM ENABLE
22
Vovp
48
50
52
4 CMP/SST
40
74
LATCH
34
LAMP ON
30
+ ERROR AMP (gm)
18
MUX
LAMP THRESH
28
MAX BRIGHT
32
46
300
2
Dim vsens
V₁<V_{DIM}<V₂
Isen3

FIG. 1

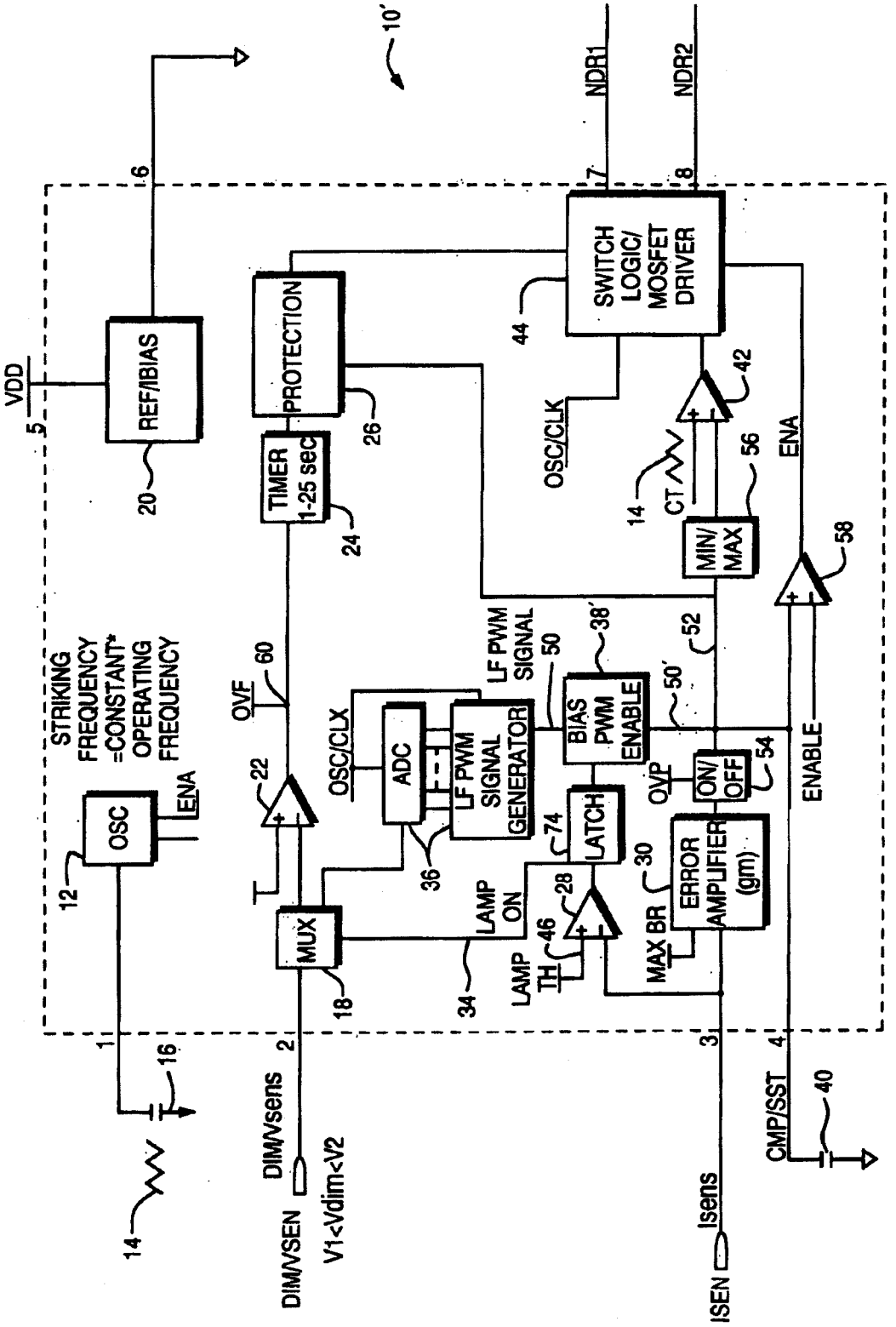

10'
NDR1
NDR2
6
7
8
SWITCH LOGIC/ MOSFET DRIVER
44
PROTECTION
26
REF/IBIAS
20
VDD
5
TIMER 1-25 sec
24
OSC/CLK
42
CT
14
56
ENA
MIN/ MAX
58
LF PWM SIGNAL
50
38'
52
50'
BIAS PWM ENABLE
OVF
60
OSC/CLX
ADC
LF PWM SIGNAL GENERATOR
22
STRIKING FREQUENCY =CONSTANT* OPERATING FREQUENCY
OSC
ENA
12
36
74
LATCH
OVP
ON/ OFF
54
ENABLE
30
ERROR AMPLIFIER (gm)
MUX
LAMP ON
28
46
LAMP TH
MAX BR
18
34
1
16
2
3
4
40
CMP/SST
DIM/Vsens
V1<Vdim<V2
DIM/VSEN
Isens
ISEN
14

FIG. 2

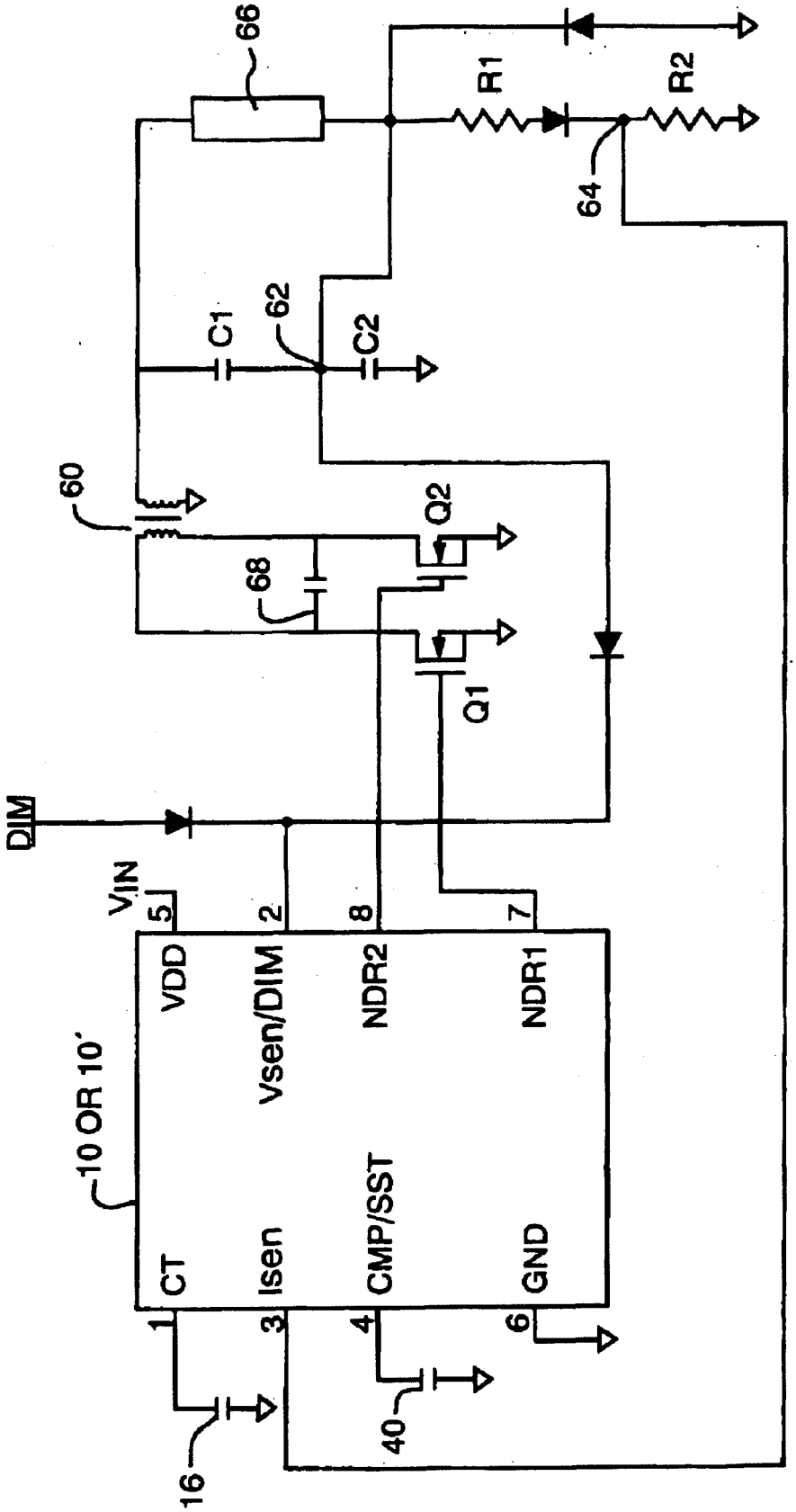

66
R1
R2
64
C1
62
C2
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen/DIM
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
16
40

FIG. 3

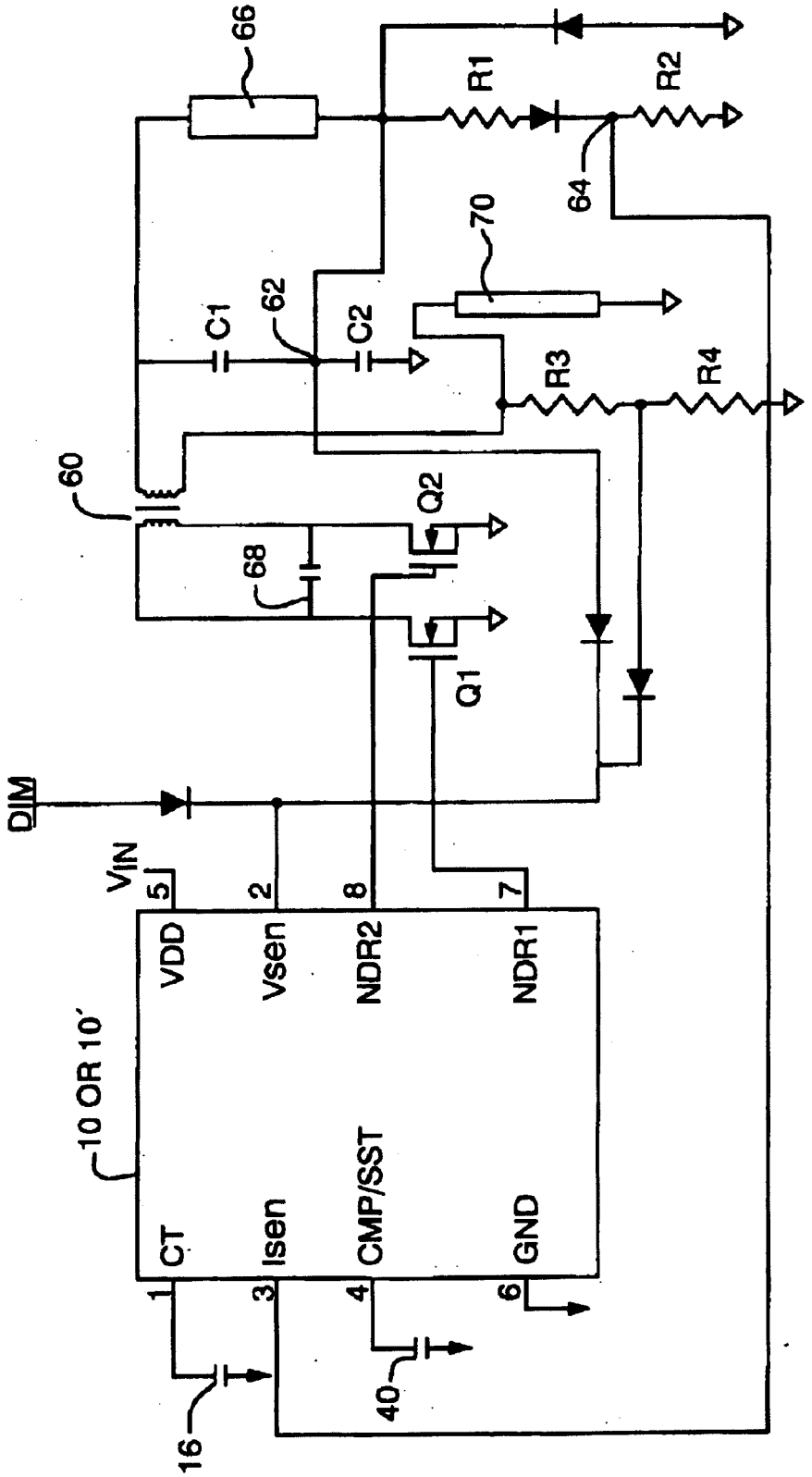

66
R1
R2
64
70
C1
62
C2
R3
R4
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
40
16

FIG. 4

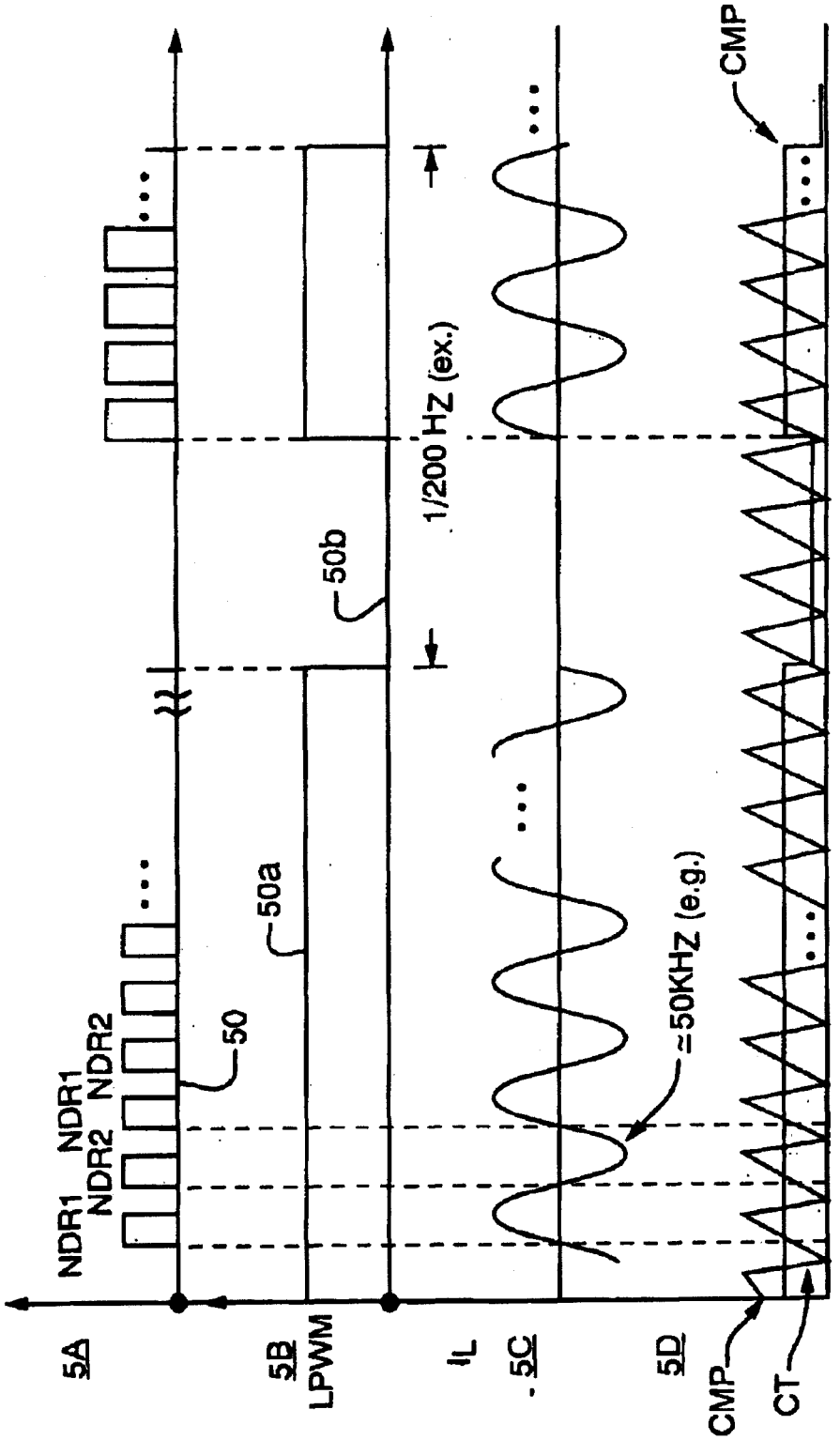

NDR1
NDR2
NDR1
NDR2
50
50a
50b
1/200 HZ (ex.)
≈50KHZ (e.g.)
CMP
5A
5B
LPWM
IL
5C
5D
CMP
CT

FIG. 5

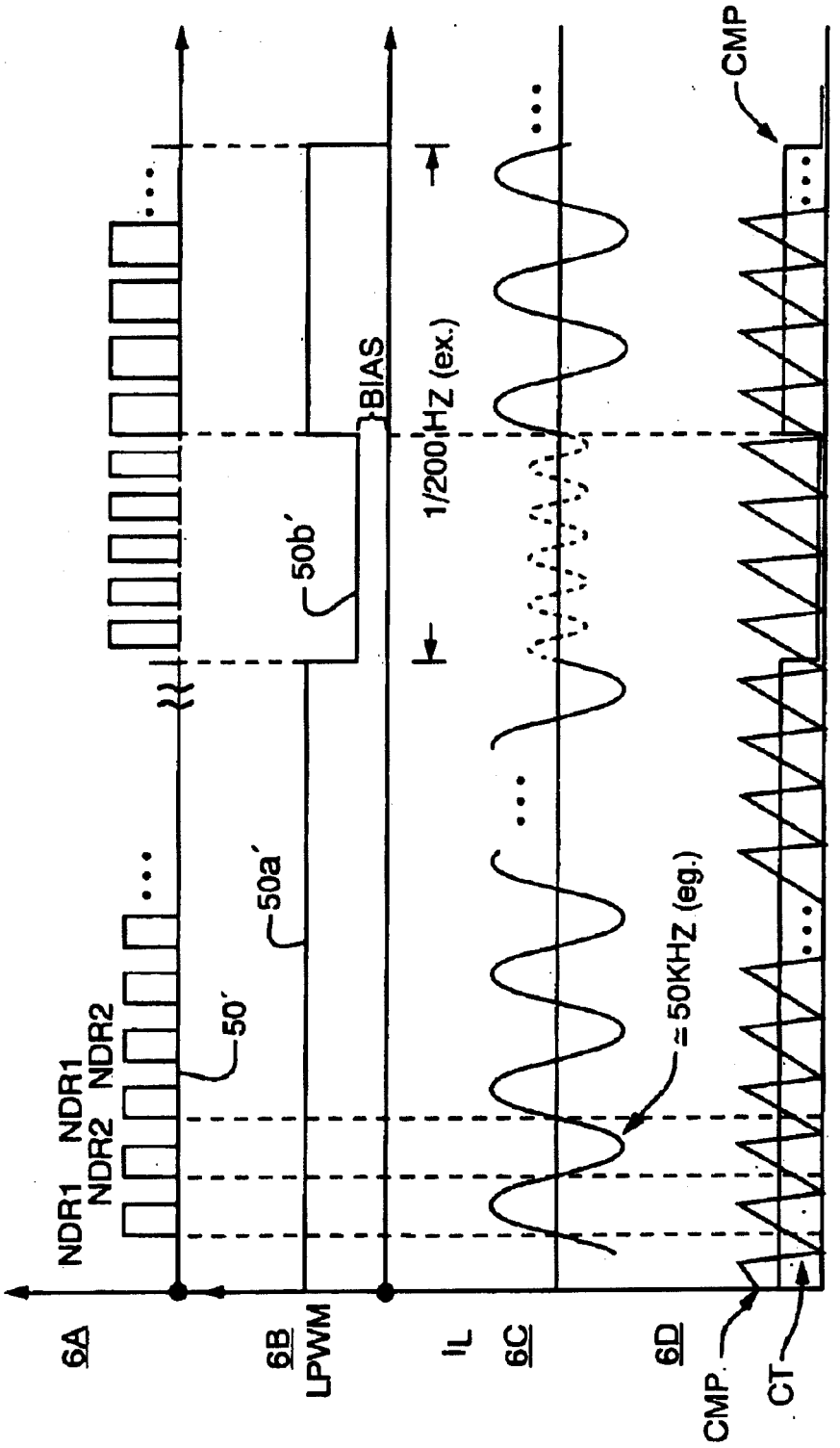

CMP
BIAS
1/200KHZ (ex.)
50b'
50a'
50'
NDR1
NDR2
NDR1
NDR2
≈50KHZ (eg.)
6A
6B
LPWM
IL
6C
6D
CMP
CT

FIG. 6

INVERTER CONTROLLER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 10/139,619, filed May 6, 2002 now U.S. Pat. No. 6,856,519.

FIELD OF THE INVENTION

The present invention relates to an inverter controller, and more particularly, to an inverter controller that utilizes pin multiplexing and/or pin multitasking techniques to reduce the overall pin count and reduce the number of components, without reducing the functionality and/or performance of the controller. Particular utility for the present invention is for a two-switch DC/AC inverter topology for driving a CCFL, however, other inverter topologies and/or DC/DC converter topologies, and/or other loads are equally contemplated herein.

SUMMARY OF THE INVENTION

The present invention provides an integrated circuit that includes an inverter controller being adapted to generate a plurality of signals to drive an inverter circuit. The controller also includes one or more input pins configured to receive two or more input signals. Each signal supports an associated function of the controller.

In one exemplary embodiment, the input pin is configured to receive a first signal representing a dim voltage, where the first signal has a first voltage range. The pin is also configured to receive a second signal representing a voltage feedback signal, where the second signal has a second voltage range.

In another exemplary embodiment, the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period. The pin is also configured to receive a second signal representing a soft start signal, where the second signal is present in a second time period.

The present invention also provides an inverter controller IC that includes a multiplexer circuit to direct one input signal to a first circuit to support a first function of the controller, and to direct another of the input signals to a second circuit to support a second said function of the controller.

The present invention further provides an inverter controller IC that includes an input pin configured to receive two or more input signals, each signal supports an associated function of the controller. One of the input signals is present in a first time period and another of the input signals is present in a second time period.

Thus, according to the present invention pin count may be significantly reduced. Also, by choosing which pins may be multifunctional and/or multiplexed, the present invention decreases tooling and PCB layout requirements.

Additional benefits and advantages of the present invention will become apparent to those skilled in the art to which this invention relates from the subsequent description of the preferred embodiments and the appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of one exemplary inverter controller integrated circuit according to the present invention;

FIG. **2** is a block diagram of another exemplary inverter controller integrated circuit according to the present invention;

FIG. **3** depicts an exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **4** depicts another exemplary application circuit topology for the inverter controller IC of FIG. **1** or **2**;

FIG. **5** depicts representative signal graphs for certain signals generated by the controller of FIG. **1**; and

FIG. **6** depicts representative signal graphs for certain signals generated by the controller of FIG. **2**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** depicts a block diagram of an exemplary inverter controller integrated circuit **10** according to the present invention. In this exemplary embodiment, the controller **10** is an **8** pin design (labeled **1–8**), where pin **2** is adapted to receive two signals and multiplexed to support two functions, and pin **4** is adapted to receive two signals to support two functions, depending on the state of certain components of the controller. In this example, pin **2** supports both load voltage sensing and dim signal sensing. Pin **4** supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

The controller **10** includes an overvoltage protection circuit **100**, a dimming circuit **200**, a current feedback control circuit **300** and an output circuit **400**. The controller **10** also includes a MUX **18** to control switching of the function of PIN **2** between load voltage sensing and dimming signal input control, based on the state of the load. The controller also includes an oscillator circuit **12** that generates a sawtooth signal **14** by charging/discharging a fixed capacitor CT **16**, and a reference signal/bias signal generator **20** that generates one or more of the reference and/or bias signals utilized by the controller **10**. The controller operates to generate two switch driving signals NDR1 and NDR2. The drive control signals may be used to drive the two switches of a derived Royer circuit, a push pull circuit, a half bridge circuit or other two-switch inverter circuit known in the art.

Stated another way, the present invention provides an inverter controller that includes a one or more multiplexed and/or multifunctional pins, where the controller is adapted to generate one or more control signals based on the signal state of the multiplexed and/or multifunctional pins. The following description of the overvoltage protection circuit **100**, the dimming circuit **200**, the current control circuit **300** and the output circuit **400** will be readily understood by those skilled in the inverter arts. Each of the components of the controller **10** is described in greater detail below.

Output circuit **400** includes a comparator **42** that compares a signal **52** from the output of the error amplifier **30** with a sawtooth signal generated by the oscillator circuit **12**. The error signal **52** is generated by the current control circuit **300** and/or the CMP capacitor **40** (at PIN **4**), as also may be modified by the dimming circuit **200**. The error signal has a value to be within the range of the minimum and maximum value of the sawtooth signal **14** for normal operation. For example, for CCFL loads, the sawtooth signal may have a range between 0V and 3.0V. As is understood in the art, the intersection between the sawtooth signal **14** and the error signal **52** is used by the switch driver logic **44** to set the pulse width of each of the switch driver signals NDR1 and NDR2. Generally, the higher the error signal value, the wider the

pulse width and thus, more power is delivered to the load (although the circuitry could be modified where the reverse is true).

As set forth above, the value of the error signal **52** is determined by current feedback information generated by the current control circuit **300**, and modified by the dimming circuit **200**. As a general matter, The CMP capacitor **40** is charged during the initial power on of the controller **10**. Error amplifier **30** operates as a current source (e.g., transconductance amplifier) to adjust the charge on the CMP capacitor **40**. Amplifier **30** compares the load current Isens to a user-definable reference signal **32** indicative of maximum load current at maximum power or maximum brightness **32**. If the value of the load current is less than signal **32**, amplifier **30** will source current to charge the capacitor **40** in an attempt to increase the DC value of the error signal **52**, thereby increasing the pulse width of the output driver signals NDR1 and NDR2. If the value of the load current is greater than the reference signal **32**, amplifier **30** will sink charge from the CMP capacitor **40** to decrease the DC value of the error signal **52**, thereby decreasing the pulse width of the output driver signals NDR1 and NDR2. In other words, amplifier **30** represents a closed loop feedback current control that sources or sinks current to attempt to maintain the load current Isens approximately equal to the reference signal **32**.

Dimming circuitry **200** is enabled by the MUX circuit **18** (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN **2**). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry **200** is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal **50**) that's duty cycle is proportional to Vdim. The frequency of the burst mode signal **50** is selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35–80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

In the exemplary embodiment, dimming circuit **200** comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit **36** generates a burst mode signal **50** that has a duty cycle proportional to the value of Vdim. In this example, the duty cycle of the burst mode signal **50** ranges from 0% (Vdin=V1) to 100% (Vdim=V2).

If the dimming circuit **200** is enabled by the MUX **18**, the PWM enable block **38** operates to sink charge from the CMP capacitor **40**. The enable block **38** may comprise a simple switch tied to ground whose conduction state is controlled by the burst mode signal **50**. As stated above, error amplifier **30** generates an output to maintain a DC signal **52** having a maximum value represented by signal **32**. The burst mode signal **50** operates as follows. When the burst mode signal is asserted (high or low), the enable circuit **38** sinks the charge from the capacitor **40**. The resulting DC signal **52** is a minimum value (e.g., 0 Volts). As a result, the signal generated by comparator **42** represents the intersection between the lowest value of the CT signal **14** and the DC signal **52**, and accordingly the switch driver logic **44** turns the driving signals NDR1 and NDR2 off while the burst mode signal is asserted. When the burst mode signal is deasserted, the PWM enable block essentially becomes an open circuit and the error amplifier **30** recharges capacitor **40** to the original value. The resulting error signal resumes to the value corresponding to the maximum brightness output as described above, and accordingly the switch logic driver generates driving signals NDR1 and NDR2 having a duty cycle corresponding to the maximum brightness output. Thus, burst mode operation, in this exemplary embodiment swings the output from fully on to fully off at a frequency determined by the burst mode signal **50**.

PIN **2** is adapted to receive two signals representing both load voltage sensing (Vsens) and DIM signal input. The DIM signal (Vdim) is used to support power control of the load. Load voltage control is used, for example, to detect an overvoltage condition at the load. In this example, a multiplexer MUX **18** is ustilized to direct the input on PIN **2** (either Vsens or Vdim) into the overvoltage protection circuit **100** or the dimming circuit **200**, based on a predetermined condition. In this example, the predetermined condition is a lamp on signal **34** which indicates that a lamp load is present and working properly, where signal **34** is an input to the MUX **18**. In this exemplary embodiment, the DIM signal is fixed to a predetermined range, i.e., V1<Vdim<V2. Vsens is configured to be outside this range, i.e., Vsens>V2, or Vsens<V1.

When the controller is initially powered on to drive a load, the controller will receive both load voltage and load current feedback to determine if the load is operating properly. Current feedback is represented by Isens at PIN **3**, and voltage feedback is represented by Vsens at PIN **2**. Assuming a lamp load (e.g., CCFL), those skilled in the art will recognize that a broken or missing lamp can create a dangerously high voltage situation at the secondary side of a transformer (not shown in FIG. **1**). Thus, the present invention initially determines the status of the lamp load by checking if a minimum current is being delivered to the load.

To that end, comparator **28** compares the load current Isens with a lamp threshold signal **46**. The lamp threshold signal **46** is a signal indicative of the minimum current that should be present at the load if the load is working properly. If Isens is greater than or equal to signal **46**, comparator **28** generates a lamp on signal **34** indicative that the load is properly working. The lamp on signal **34** is a control signal generated by the comparator **28** that controls the state of the MUX **18**. In this case, the lamp on signal sets the output state of the MUX to couple the dimming circuitry **200** to PIN **2**. A latch circuit **74** is provided to latch the output of the lamp on signal once Isens exceeds the threshold signal **46**. The lamp on signal will remain in this state during normal operation, so that burst mode dimming (described below) does not change the state of the lamp on signal. The Vdim input on PIN2 is then used to set the desired dim brightness value (as will be described below).

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit **74** is set), the current sense value Isens stays below the lamp threshold signal **46**, the output of the amplifier **28** changes the state of the lamp on signal **34**. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit **100** to PIN **2**. As is understood in the CCFL arts, Veens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however, and open or broken lamp condition exists, Vsens will rise to a value greater than V2.

When PIN **2** is coupled to the overvoltage protection circuit **100**, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in comparator **22**. When Vseria exceeds Vovp **48**. the output of comparator causes timing circuit **24** to initiate a predefined timeout period.

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal **46**. Also, error amplifier **30** will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the timeout period, the protection circuit operates in a manner similar to the PWM enable circuit **38**. During this period, to prevent the error amplifier from generating a error signal to cause the switches to drive at higher power, the OVP signal **60** stops the error amplifier **30** to charge/discharge of CMP capacitor **40**. At the end of the timeout, the protection circuit **26** disables the switch driver logic **44** and thus the output overvoltage is controlled.

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit **100** configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit **200** configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit **300** configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit **400** configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN **2**) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer **18** is coupled to the pin and configured to direct the voltage feedback signal to the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

PIN **4** and the CMP capacitor also operates to control soft start (SST) functionality. Soft start, as is known in the art, essentially operates in the beginning of power on, to cause the output circuitry to generate a minimal pulse width and gradually increase the pulse width. At initial power on the voltage on the CMP capacitor is zero. Isens is also zero, and therefore the error amplifier attempts to source the CMP capacitor to a charge that satisfies signal **32**. The time this process takes is dependent on the desired charge on CMP and the capacitance of CMP, and therefore this time period is utilized as soft start. This ensures that the amount of power to the load is increased gradually. It continues until the load current value reaches the threshold value **32**. Then the error amplifier **30** takes over the control of PIN **4** which is the charge on the capacitor, as described herein. For CCFL loads, it is known that a gradual increase in lamp current helps to ensure the life of the lamp.

Thus, PIN **4** is adapted to generate the DC signal CMP **52** based on the values of the error signal generated by the current control circuit **300** and/or the dimming signal generated by the dimming circuit **200**. PIN **4** is multifunctional since it is also adapted to generate a soft start signal **52** based on the value of the error signal generated by the current control circuit **300**.

FIG. **5** depicts representative signal graphs for certain signals generated by the controller **10** of the present invention. FIG. **5A** shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **5D**. FIG. **5B** depicts the burst mode signal (LPWM) **50**, and FIG. **5C** depicts the load current I_L. When the burst mode signal is deasserted (high) **50A**, the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50B**, the drive signals stop and the lamp current is approximately zero. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (approximately zero) as described above.

FIG. **2** depicts another exemplary inverter controller **10'** according to the present invention. The inverter controller **10'** of this exemplary embodiment operates in a similar manner as described above with reference to FIG. **1**, but includes additional circuitry which may be desirable for a given operating environment. For example, at the output of error amplifier **30** is an on/off circuit triggered by the OVP signal. If the overvoltage protection circuit is activated, the OVP signal shuts the output of the error amplifier **30** off; regardless of the value of Isens. Thus, when the OVP signal is asserted, capacitor **40**. Of course, the protection circuitry may also be adapted to charge or discharge the capacitor **40** to some minimum level so that the output signals deliver a predetermined minimum pulse width to the load during the time out period.

The controller **10'** also includes a mm/max circuit **56** which, during times when the burst mode signal is enabled, generates a minimum DC value (instead of a zero DC value **52**, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the nun/max circuit **56** generates an output to cause the output signals to have same predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintain a continuous function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

An enable comparator **58** is provided to generate an enable control signal to the switch logic **44**. The comparator generates an enable signal (thereby enabling the switch logic) if the value on the capacitor **40** is greater than the enable threshold value or else the switch logic is disabled.

The PWM enable circuit **38'** may include a floor value (i.e., bias), below which the PWM enable circuit will not sink charge from the CMP capacitor **40**. Like the min/max circuit, this prevents the burst mode enabled signal from completely sinking the charge on the capacitor, so that the output signals are set at a predetermined minimum other than zero. The value of the bias may be selected in accordance with the operating range of the controller, a desired minimum power delivered to the load during burst mode assertion, and/or other factors that will be apparent to those skilled in the art.

FIG. **6** depicts representative signal graphs for certain signals generated by the controller **10'** of the present invention. FIG. **6A** shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **6D**. FIG. **6B** depicts the burst mode signal (LPWM) **50'**, and FIG. **6C** depicts the load current I_L. When the burst mode signal is deasserted (high) **50A'**, the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50B'**, the drive signals are reduced to a predetermined minimum pulse width and the lamp current is significantly. reduced. The asserted value of the burst mode signal **50B'** is biased in a manner described above. Note that when the burst mode

signal is asserted the CMP signal drops to a minimum value (greater than zero), as described above.

Thus, the exemplary inverter controller ICs **10** and **10'** of FIGS. **1** and **2** include a pin (e.g., PIN2) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverted controller ICs **10** and **10'** are also adapted to include a pin (e.g., PIN **4**) that is multifunctional to operate in a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

FIG. **3** depicts an exemplary application topology for the inverter controller IC **10** or **10'**. The controller IC **10** or **10'** depicted in FIG. **3** is used to drive a derived Royer circuit comprised of transistors Q1 and Q2, to power a CCFL load **66**. Q1 and Q2 drive the primary side of the transformer **60**, through a resonant tank circuit formed by the capacitor **68** and the primary side inductance of the transformer **60**. The operation of this type of circuit is well known by those skilled in the art. Vsen is derived from a voltage divider between capacitors C1 and C2 (node **62**) so that the value of Vsen is nominal compared to the voltage at the secondary side of the transformer. Vsen is typically in the range of 1 to 5 Volts. Isen is derived from the CCFL load through the divider circuit of R1 and R2 (node **64**). Isen will typically range between 0 Volts (no lamp) to 1.25 Volts (full lamp brightness). Of course, these values are only exemplary, and may be modified to meet design criteria without departing from the present invention. FIG. **4** represents another exemplary application topology for the inverter controller **10** or **10'**. The controller in this embodiment is used to drive two (or more) CCFL loads **66** and **70**. In this case, since lamps **66** and **70** are in series, current feedback Isens is derived from the voltage divider R1, R2.

Those skilled in the art will recognize numerous modifications that may be made to the present invention. For example, the controller ICs **10** and **10'** of FIGS. **1** and **2** multiplex the values of Vsen and DIM on PIN **2**, and combine the functionality of the charge capacitor CMP **40** and soft start functionality. However, these are only examples of pin multiplexing/multitasking that may be accomplished by the present invention. Other pins associated with the exemplary IC may be multiplexed and/or multitasked. Additionally, other IC designs that require more or fewer pins than the 8 pin IC depicted in FIGS. **1** and **2** may likewise include pin multitasking and/or multiplexing as provided herein.

Still other modifications may be made. In the exemplary controller ICs of FIGS. **1** and **2**, PIN **2** is multiplexed to support both load voltage sensing and dim signal input. The range of dim signals (V1<Vdim<V2), as disclosed above, and the overvoltage protection threshold Vovp are selected such that Vovp>V2. However, this relationship is not required for the present invention to operate properly. Indeed Vovp may be selected within or below the range of Vdim, since the Vdim value is used by the overvoltage protection circuit **100**, independent of the dim value. Alternatively, the multiplexed and/or multifunctional pins disclosed herein may be adapted to support three or more signals, using multiplexing and or multifunctional techniques provided herein.

Still other modifications may be made. For example, the exemplary application topologies of FIGS. **3** and **4** depict the controller ICs **10** or **10'** driving a derived Royer circuit formed by Q1 and Q2. However, the controller **10** or **10'** may be likewise applied to a push-pull inverter, a half bridge inverter and/or other type of two switch inverter topology known in the art. Yet further, the controller IC **10** or **10'** may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC **10** or **10'** to drive a four switch inverter topology (e.g., full bridge inverter).

The present invention is not limited to a CCFL load. Indeed the controller **10** or **10'** of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller **10** or **10'** of the present invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the loud type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in FIG. **4**, numerous other topologies may be used, for example as described in U.S. Pat. No. 6,104,146, and U.S. patent application Ser. Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are incorporated by reference in their entirety.

A detailed discussion of the operation of certain components of FIGS. **1** and **2** has been omitted. For example, the operation of the oscillator circuit **12** and the operation of the switch logic **44** have been omitted since it is assumed that one skilled in the art will readily recognize both the operation and implementation of these features. Also, the timing of the drive signals NDR1 and NDR2 is not described at length herein, since the operation of these signals will be apparent to those skilled in the art. The preceding detailed description of the block diagrams of FIGS. **1** and **2** is largely directed to the functionality of the components. The components of FIGS. **1** and **2** may be off-the-shelf or custom components to achieve the functionality stated herein, and those skilled in the art will readily recognize that many circuit implementations may be used to accomplish the functionality stated herein, and all such alternatives are deemed within the scope of the present invention.

Still further, inverter controller circuits that include voltage and current feedback, and dimming control (as described herein) are well known to those skilled in the art. However, the prior art integrated circuit inverter controllers have failed to address the long-felt need to reduce the IC package pin count while maintaining the functionality of the inverter IC. The present invention described herein provides examples of addressing this issue by providing, for example, multiplexed and/or multifunctional IC pins. Numerous modifications to this inventive theme will be apparent to those skilled in the art, and all such modifications are deemed within the scope of the present invention, as set forth in the claims.

What is claimed is:

1. A computer system, comprising:

one or more cold cathode fluorescent lamps (CCFLs);

an inverter circuit capable of generating an AC signal to power said one or more lamps; and

an inverter controller capable of controlling said inverter circuit, said controller comprising a first-input pin capable of receiving a first input signal representing a current feedback signal and a second input signal representing a soft start signal, each said input signal supporting an associated function of said controller during operation of said controller.

2. A computer system as claimed in claim **1**, wherein said inverter circuit selected from a push-pull, half bridge and full-bridge inverter topologies.

3. A computer system as claimed in claim 1, wherein said inverter circuit comprises a plurality of power switches for converting a DC signal to said AC signal.

4. A computer system as claimed in claim 1, wherein said inverter circuit comprises a step-up transformer receiving said AC signal and generating a stepped-up AC signal.

5. A computer system as claimed in claim 1, wherein said controller further comprising a second input pin, said second input pin configured to receive a third signal representing a dim voltage, said third signal having a first voltage range; and a fourth signal representing a voltage feedback signal indicative of voltage supplied to said CCFL, said fourth signal having a second voltage range.

6. A computer system as claimed in claim 5, further comprising a multiplexer circuit to direct one of said third or fourth signals to a first circuit to support a function of said controller, and to direct another of said third or fourth signals to a second circuit to support another function of said controller.

7. A computer system as claimed in claim 1, wherein one of said first or second signals is present in a first time period and another of said first or second signals is present in a second time period.

* * * * *

EXHIBIT D

US007120035B2

(12) **United States Patent**
Lin et al.

(10) **Patent No.: US 7,120,035 B2**
(45) **Date of Patent: *Oct. 10, 2006**

(54) **INVERTER CONTROLLER**

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(73) Assignee: **O2Micro International Limited**, Grand Cayman (KY)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **10/690,103**

(22) Filed: **Oct. 21, 2003**

(65) **Prior Publication Data**

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Related U.S. Application Data

(62) Division of application No. 10/139,619, filed on May 6, 2002, now Pat. No. 6,856,519.

(51) **Int. Cl.**
H02M 3/335 (2006.01)

(52) **U.S. Cl.** **363/16**; 363/132; 315/307; 323/905

(58) **Field of Classification Search** 363/17, 363/131, 132, 25, 56.05, 56.11, 56.01; 323/905; 315/306, 307; 713/1; 710/5, 36
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,527,126 A	7/1985	Petrich et al.	.....	328/155
5,615,093 A *	3/1997	Nalbant	.....	363/25
5,859,768 A	1/1999	Hall et al.	.....	363/21
6,198,236 B1 *	3/2001	O'Neill	.....	315/307
6,567,866 B1 *	5/2003	Poisner	.....	710/36
6,640,271 B1 *	10/2003	Ehrenhardt et al.	.....	713/1

FOREIGN PATENT DOCUMENTS

JP	05028276	2/1993
JP	H06-196290	7/1994
JP	06266576	9/1994
WO	WO 00/40062	7/2000
WO	WO 01/95332	12/2001

OTHER PUBLICATIONS

Decision of Rejection, with English translation, received in related Japanese Application (3 pgs).
Taiwan Office Action from related Taiwan application, dated Oct. 18, 2004, with English translation.

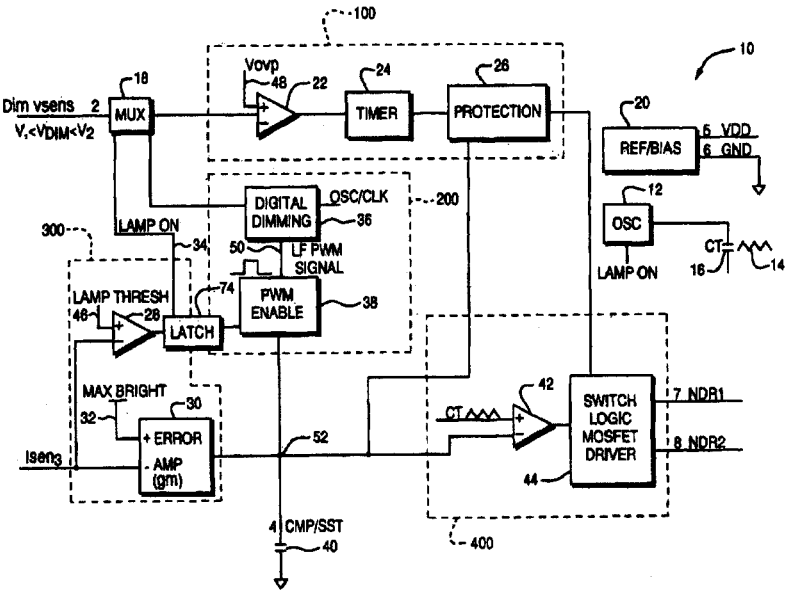
* cited by examiner

Primary Examiner—Jessica Han
(74) *Attorney, Agent, or Firm*—Grossman, Tucker, Perreault & Pfleger PLLC

(57) **ABSTRACT**

An integrated circuit inverter controller that includes at least one input pin that is configured to receive two or more input signals. The input pin may be multiplexed so that the appropriate input signal is directed to appropriate circuitry within the controller to support two or more functions of the controller. Alternatively, the input signals may be present in differing time periods so that a single pin can support two or more functions. Multifunctional or multitasked pins reduce the overall pin count of the inverter controller.

10 Claims, 6 Drawing Sheets



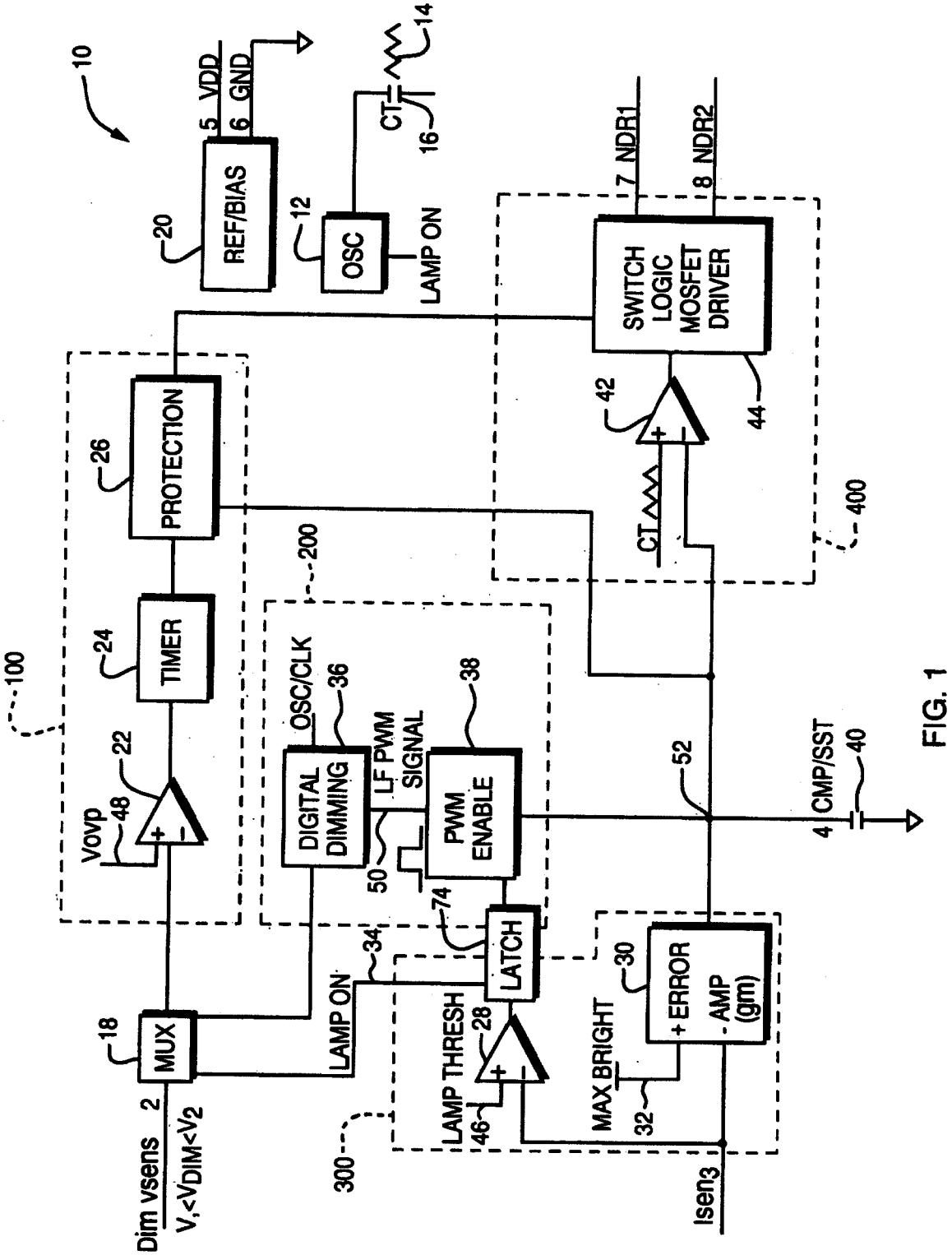

10
5 VDD
6 GND
14
CT
16
20
REF/BIAS
12
OSC
LAMP ON
7 NDR1
8 NDR2
SWITCH LOGIC MOSFET DRIVER
42
44
26
PROTECTION
CT
400
200
24
TIMER
100
OSC/CLK
36
38
22
DIGITAL DIMMING
LF PWM SIGNAL
PWM ENABLE
52
4 CMP/SST
40
Vovp
48
50
74
LATCH
34
LAMP ON
30
+ ERROR - AMP (gm)
18
MUX
28
LAMP THRESH
MAX BRIGHT
2
Dim vsens
$V_1 < V_{DIM} < V_2$
46
32
300
Isen3

FIG. 1

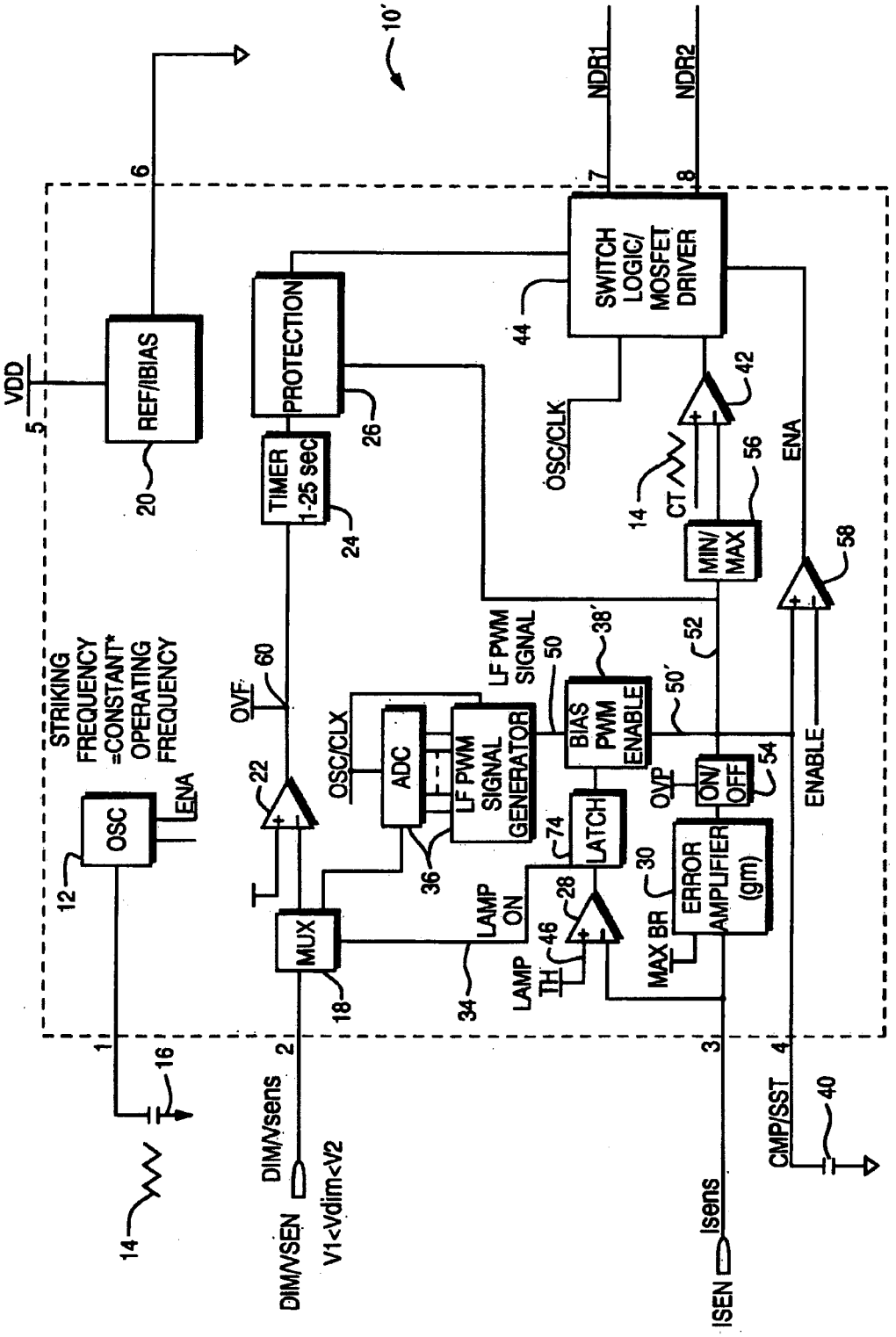

10'
NDR1
NDR2
6
7
8
SWITCH LOGIC/ MOSFET DRIVER
44
PROTECTION
26
REF/IBIAS
20
VDD
5
TIMER 1-25 sec
24
OSC/CLK
42
CT
14
56
ENA
MIN/ MAX
58
LF PWM SIGNAL
50
38'
52
50'
BIAS PWM ENABLE
OVF
60
OSC/CLX
ADC
LF PWM SIGNAL GENERATOR
STRIKING FREQUENCY =CONSTANT* OPERATING FREQUENCY
OSC
ENA
12
22
36
74
LATCH
OVP
ON/ OFF
54
ENABLE
ERROR AMPLIFIER (gm)
30
LAMP ON
28
MUX
18
34
LAMP TH
46
MAX BR
1
16
2
DIM/Vsens
3
4
CMP/SST
40
14
DIM/VSEN
V1<Vdim<V2
Isens
ISEN

FIG. 2

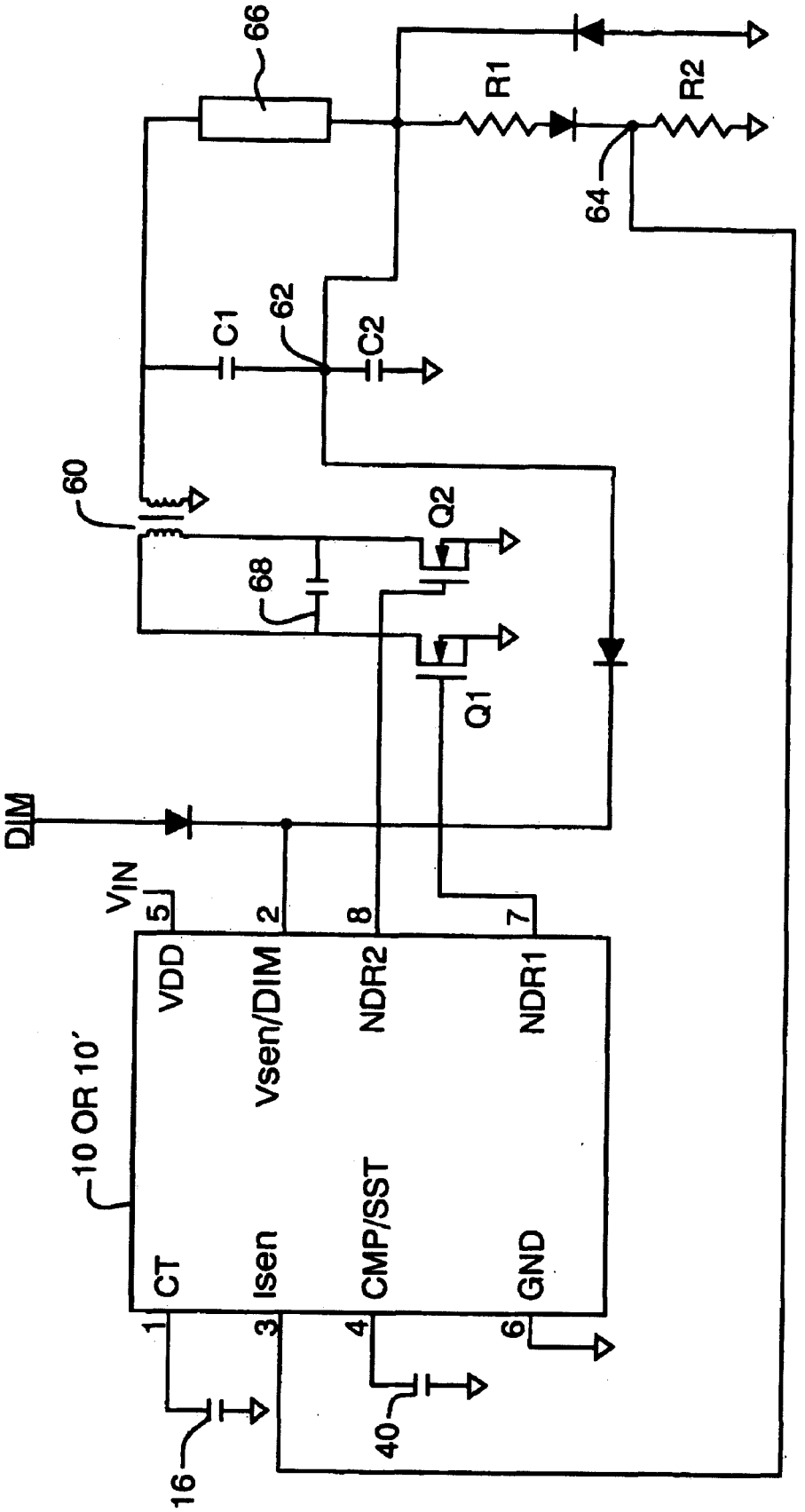

66
R1
R2
64
C1
62
C2
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen/DIM
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
16
40

FIG. 3

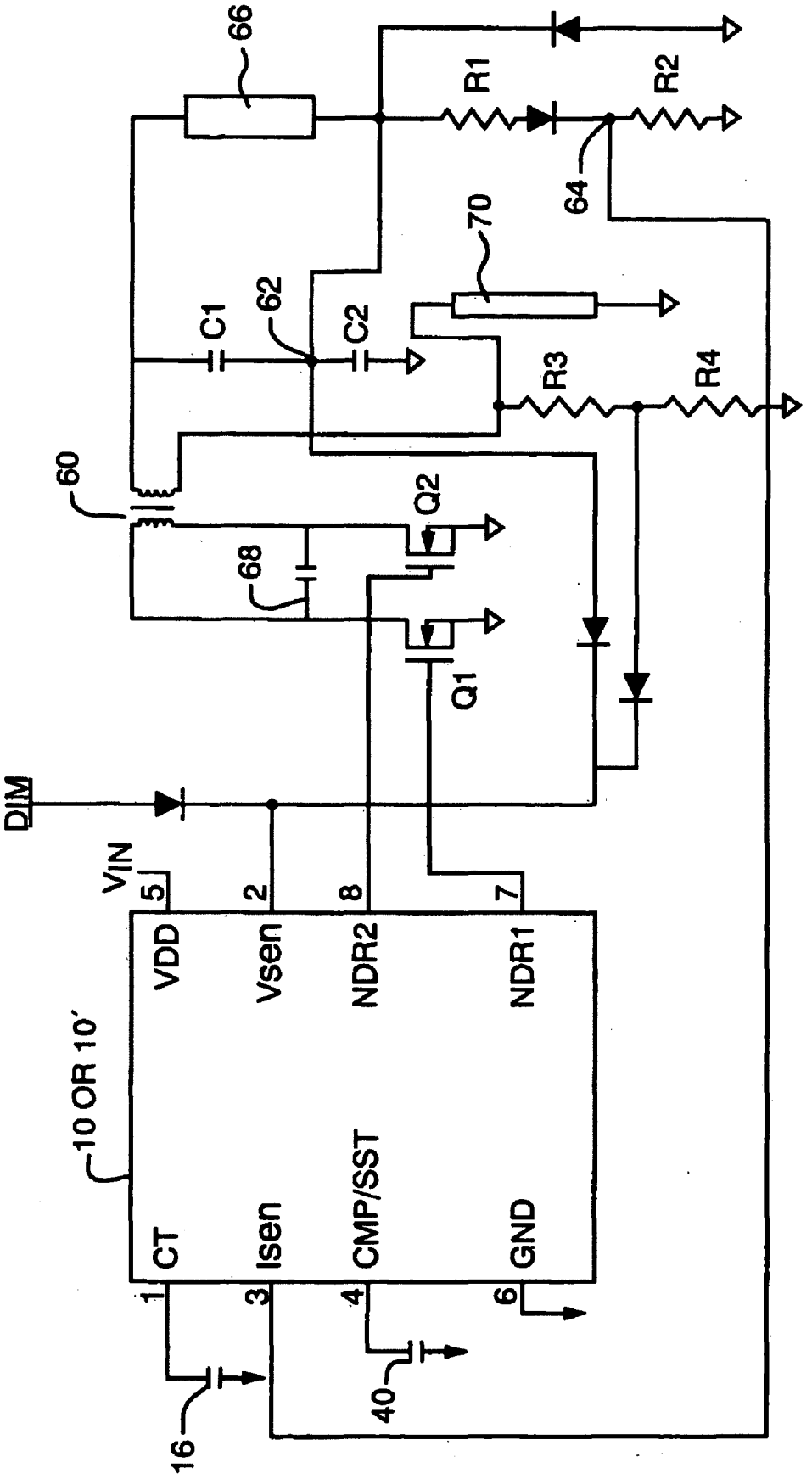

66
R1
R2
64
70
C1
62
C2
R3
R4
60
Q2
68
Q1
DIM
VIN
5
2
8
7
VDD
Vsen
NDR2
NDR1
10 OR 10'
CT
Isen
CMP/SST
GND
1
3
4
6
40
16

FIG. 4

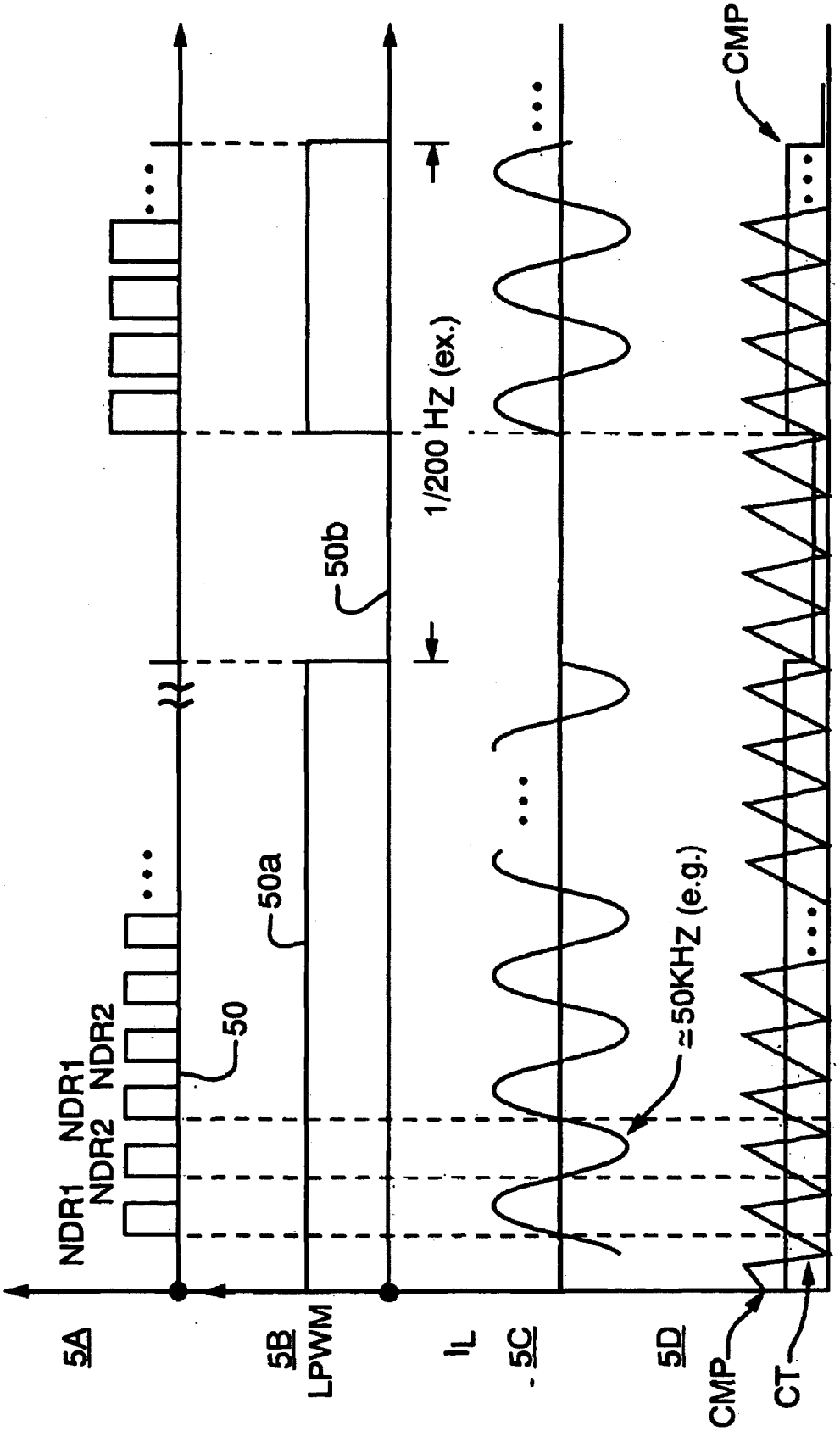

5A
NDR1
NDR2
NDR1
NDR2
50
50a
5B
LPWM
50b
1/200 HZ (ex.)
IL
5C
≃50KHZ (e.g.)
5D
CMP
CT
CMP

FIG. 5

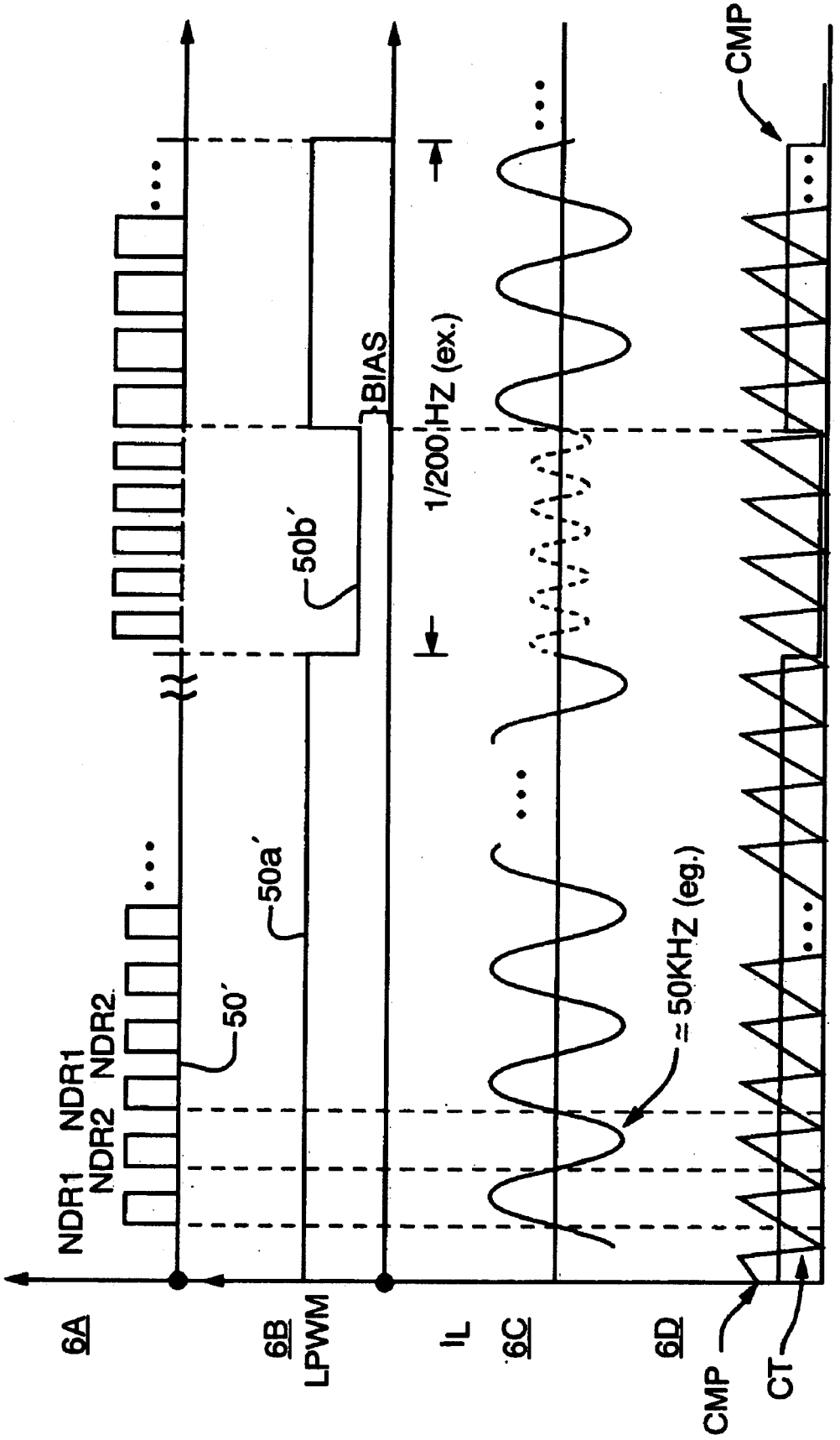

NDR1
NDR2
NDR1
NDR2
50'
50a'
50b'
BIAS
1/200 HZ (ex.)
≈ 50KHZ (eg.)
CMP
6A
6B
LPWM
IL
6C
6D
CMP
CT

FIG. 6

INVERTER CONTROLLER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. patent application Ser. No. 10/139,619, filed May 6, 2002 now U.S. Pat. No. 6,856,519.

FIELD OF THE INVENTION

The present invention relates to an inverter controller, and more particularly, to an inverter controller that utilizes pin multiplexing and/or pin multitasking techniques to reduce the overall pin count and reduce the number of components, without reducing the functionality and/or performance of the controller. Particular utility for the present invention is for a two-switch DC/AC inverter topology for driving a CCFL, however, other inverter topologies and/or DC/DC converter topologies, and/or other loads are equally contemplated herein.

SUMMARY OF THE INVENTION

The present invention provides an integrated circuit that includes an inverter controller being adapted to generate a plurality of signals to drive an inverter circuit. The controller also includes one or more input pins configured to receive two or more input signals. Each signal supports an associated function of the controller.

In one exemplary embodiment, the input pin is configured to receive a first signal representing a dim voltage, where the first signal has a first voltage range. The pin is also configured to receive a second signal representing a voltage feedback signal, where the second signal has a second voltage range.

In another exemplary embodiment, the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period. The pin is also configured to receive a second signal representing a soft start signal, where the second signal is present in a second time period.

The present invention also provides an inverter controller IC that includes a multiplexer circuit to direct one input signal to a first circuit to support a first function of the controller, and to direct another of the input signals to a second circuit to support a second said function of the controller.

The present invention further provides an inverter controller IC that includes an input pin configured to receive two or more input signals, each signal supports an associated function of the controller. One of the input signals is present in a first time period and another of the input signals is present in a second time period.

Thus, according to the present invention pin count may be significantly reduced. Also, by choosing which pins may be multifunctional and/or multiplexed, the present invention decreases tooling and PCB layout requirements.

Additional benefits and advantages of the present invention will become apparent to those skilled in the art to which this invention relates from the subsequent description of the preferred embodiments and the appended claims, taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of one exemplary inverter controller integrated circuit according to the present invention;

FIG. **2** is a block diagram of another exemplary inverter controller integrated circuit according to the present invention;

FIG. **3** depicts an exemplary application circuit topology for the inverter controller IC of FIGS. **1** or **2**;

FIG. **4** depicts another exemplary application circuit topology for the inverter controller IC of FIGS. **1** or **2**;

FIG. **5** depicts representative signal graphs for certain signals generated by the controller of FIG. **1**; and

FIG. **6** depicts representative signal graphs for certain signals generated by the controller of FIG. **2**.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

FIG. **1** depicts a block diagram of an exemplary inverter controller integrated circuit **10** according to the present invention. In this exemplary embodiment, the controller **10** is an 8 pin design (labeled **1**–**8**), where pin **2** is adapted to receive two signals and multiplexed to support two functions, and pin **4** is adapted to receive two signals to support two functions, depending on the state of certain components of the controller. In this example, pin **2** supports both load voltage sensing and dim signal sensing. Pin **4** supports both current comparing during normal operating conditions and soft start (SST) operation during initial turn on and/or lamp out conditions.

The controller **10** includes an overvoltage protection circuit **100**, a dimming circuit **200**, a current feedback control circuit **300** and an output circuit **400**. The controller **10** also includes a MUX **18** to control switching of the function of PIN **2** between load voltage sensing and dimming signal input control, based on the state of the load. The controller also includes an oscillator circuit **12** that generates a sawtooth signal **14** by charging/discharging a fixed capacitor CT **16**, and a reference signal/bias signal generator **20** that generates one or more of the reference and/or bias signals utilized by the controller **10**. The controller operates to generate two switch driving signals NDR1 and NDR2. The drive control signals may be used to drive the two switches of a derived Royer circuit, a push pull circuit, a half bridge circuit or other two-switch inverter circuit known in the art.

Stated another way, the present invention provides an inverter controller that includes a one or more multiplexed and/or multifunctional pins, where the controller is adapted to generate one or more control signals based on the signal state of the multiplexed and/or multifunctional pins. The following description of the overvoltage protection circuit **100**, the dimming circuit **200**, the current control circuit **300** and the output circuit **400** will be readily understood by those skilled in the inverter arts. Each of the components of the controller **10** is described in greater detail below.

Output circuit **400** includes a comparator **42** that compares a signal **52** from the output of the error amplifier **30** with a sawtooth signal generated by the oscillator circuit **12**. The error signal **52** is generated by the current control circuit **300** and/or the CMP capacitor **40** (at PIN **4**), as also may be modified by the dimming circuit **200**. The error signal has a value to be within the range of the minimum and maximum value of the sawtooth signal **14** for normal operation. For example, for CCFL loads, the sawtooth signal may have a

range between 0V and 3.0V. As is understood in the art, the intersection between the sawtooth signal **14** and the error signal **52** is used by the switch driver logic **44** to set the pulse width of each of the switch driver signals NDR1 and NDR2. Generally, the higher the error signal value, the wider the pulse width and thus, more power is delivered to the load (although the circuitry could be modified where the reverse is true).

As set forth above, the value of the error signal **52** is determined by current feedback information generated by the current control circuit **300**, and modified by the dimming circuit **200**. As a general matter, The CMP capacitor **40** is charged during the initial power on of the controller **10**. Error amplifier **30** operates as a current source (e.g., transconductance amplifier) to adjust the charge on the CMP capacitor **40**. Amplifier **30** compares the load current Isens to a user-definable reference signal **32** indicative of maximum load current at maximum power or maximum brightness **32**. If the value of the load current is less than signal **32**, amplifier **30** will source current to charge the capacitor **40** in an attempt to increase the DC value of the error signal **52**, thereby increasing the pulse width of the output driver signals NDR1 and NDR2. If the value of the load current is greater than the reference signal **32**, amplifier **30** will sink charge from the CMP capacitor **40** to decrease the DC value of the error signal **52**, thereby decreasing the pulse width of the output driver signals NDR1 and NDR2. In other words, amplifier **30** represents a closed loop feedback current control that sources or sinks current to attempt to maintain the load current Isens approximately equal to the reference signal **32**.

Dimming circuitry **200** is enabled by the MUX circuit **18** (a process that is described in greater detail below), the relative dim value is set by VDIM (PIN **2**). In the exemplary embodiment, VDIM is a DC signal having a value between V1 and V2. VDIM may be generated by a software programmable dimming value or a switch (e.g., rotary switch) operated by a user. In this example, the greater the value of Vdim, the more power is delivered to the load although the circuitry could be modified where the reverse is true. Dimming circuitry **200** is a burst mode dimming circuit that generates a burst mode signal (low frequency PWM signal **50**) that's duty cycle is proportional to Vdim. The frequency of the burst mode signal **50** is selected to be far less than the frequency of the driving signals NDR1 and NDR2. For example, for CCFL applications the typical operating range of the driving signals is 35–80 kHz, and the burst mode signal may have a frequency of approximately 200 Hz.

In the exemplary embodiment, dimming circuit **200** comprises a digital dimming circuit that receives Vdim and converts Vdim to a digital signal. The digital signal is weighted to a predetermined bit depth (e.g., 8 bit) to render a predetermined number of dimming values (e.g., 256 dim levels). The digital dimming circuit **36** generates a burst mode signal **50** that has a duty cycle proportional to the value of Vdim. In this example, the duty cycle of the burst mode signal **50** ranges from 0% (Vdim=V1) to 100% (Vdim=V2).

If the dimming circuit **200** is enabled by the MUX **18**, the PWM enable block **38** operates to sink charge from the CMP capacitor **40**. The enable block **38** may comprise a simple switch tied to ground whose conduction state is controlled by the burst mode signal **50**. As stated above, error amplifier **30** generates an output to maintain a DC signal **52** having a maximum value represented by signal **32**. The burst mode signal **50** operates as follows. When the burst mode signal is asserted (high or low), the enable circuit **38** sinks the charge from the capacitor **40**. The resulting DC signal **52** is a minimum value (e.g., 0 Volts). As a result, the signal generated by comparator **42** represents the intersection between the lowest value of the CT signal **14** and the DC signal **52**, and accordingly the switch driver logic **44** turns the driving signals NDR1 and NDR2 off while the burst mode signal is asserted. When the burst mode signal is deasserted, the PWM enable block essentially becomes an open circuit and the error amplifier **30** recharges capacitor **40** to the original value. The resulting error signal resumes to the value corresponding to the maximum brightness output as described above, and accordingly the switch logic driver generates driving signals NDR1 and NDR2 having a duty cycle corresponding to the maximum brightness output. Thus, burst mode operation, in this exemplary embodiment swings the output from fully on to fully off at a frequency determined by the burst mode signal **50**.

PIN **2** is adapted to receive two signals representing both load voltage sensing (Vsens) and DIM signal input. The DIM signal (Vdim) is used to support power control of the load. Load voltage control is used, for example, to detect an overvoltage condition at the load. In this example, a multiplexer MUX **18** is utilized to direct the input on PIN **2** (either Vsens or Vdim) into the overvoltage protection circuit **100** or the dimming circuit **200**, based on a predetermined condition. In this example, the predetermined condition is a lamp on signal **34** which indicates that a lamp load is present and working properly, where signal **34** is an input to the MUX **18**. In this exemplary embodiment, the DIM signal is fixed to a predetermined range, i.e., V1<Vdim<V2. Vsens is configured to be outside this range , i.e., Vsens>V2, or Vsens<V1.

When the controller is initially powered on to drive a load, the controller will receive both load voltage and load current feedback to determine if the load is operating properly. Current feedback is represented by Isens at PIN **3**, and voltage feedback is represented by Vsens at PIN **2**. Assuming a lamp load (e.g., CCFL), those skilled in the art will recognize that a broken or missing lamp can create a dangerously high voltage situation at the secondary side of a transformer (not shown in FIG. **1**). Thus, the present invention initially determines the status of the lamp load by checking if a minimum current is being delivered to the load.

To that end, comparator **28** compares the load current Isens with a lamp threshold signal **46**. The lamp threshold signal **46** is a signal indicative of the minimum current that should be present at the load if the load is working properly. If Isens is greater than or equal to signal **46**, comparator **28** generates a lamp on signal **34** indicative that the load is properly working. The lamp on signal **34** is a control signal generated by the comparator **28** that controls the state of the MUX **18**. In this case, the lamp on signal sets the output state of the MUX to couple the dimming circuitry **200** to PIN **2**. A latch circuit **74** is provided to latch the output of the lamp on signal once Isens exceeds the threshold signal **46**. The lamp on signal will remain in this state during normal operation, so that burst mode dimming (described below) does not change the state of the lamp on signal. The Vdim input on PIN2 is then used to set the desired dim brightness value (as will be described below).

If, however, during the time when the controller is initially powered to drive the load (and before the latch circuit **74** is set), the current sense value Isens stays below the lamp threshold signal **46**, the output of the amplifier **28** changes the state of the lamp on signal **34**. This, in turn, changes the state of the MUX to couple the overvoltage protection circuit **100** to PIN **2**. As is understood in the CCFL arts,

Vsens is derived from the secondary side of the transformer used to drive the lamp load. Under normal operating conditions, Vsens will not affect the range of Vdim, i.e., V1<Vdim<V2. If, however, and open or broken lamp condition exists, Vsens will rise to a value greater than V2. When PIN **2** is coupled to the overvoltage protection circuit **100**, Vsens is compared to a predetermined overvoltage threshold signal Vovp (where Vovp>V2) in comparator **22**. When Vsens exceeds Vovp **48**, the output of comparator causes timing circuit **24** to initiate a predefined timeout period.

Since this is a broken or missing lamp condition, Isens will have a value less than the lamp threshold signal **46**. Also, error amplifier **30** will generate an output signal in an attempt to source the CMP capacitor to increase the power delivered to the load. Accordingly, during the timeout period, the protection circuit operates in a manner similar to the PWM enable circuit **38**. During this period, to prevent the error amplifier from generating a error signal to cause the switches to drive at higher power, the OVP signal **60** stops the error amplifier **30** to charge/discharge of CMP capacitor **40**. At the end of the timeout, the protection circuit **26** disables the switch driver logic **44** and thus the output overvoltage is controlled.

Thus, to summarize, the present invention provides an inverter controller IC for generating power to a load that includes: 1) an overvoltage protection circuit **100** configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load, 2) a dimming circuit **200** configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load, 3) a current control circuit **300** configured to receive a current feedback signal from the load and configured to generate an error signal; and an output circuit **400** configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load. One of the IC pins (e.g., PIN **2**) is configured to receive the voltage feedback signal and the dimming signal. A multiplexer **18** is coupled to the pin and configured to direct the voltage feedback signal to the overvoltage protection circuit or the dimming signal to the dimming circuit, based on the value of the current feedback signal.

PIN **4** and the CMP capacitor also operates to control soft start (SST) functionality. Soft start, as is known in the art, essentially operates in the beginning of power on, to cause the output circuitry to generate a minimal pulse width and gradually increase the pulse width. At initial power on the voltage on the CMP capacitor is zero. Isens is also zero, and therefore the error amplifier attempts to source the CMP capacitor to a charge that satisfies signal **32**. The time this process takes is dependent on the desired charge on CMP and the capacitance of CMP, and therefore this time period is utilized as soft start. This ensures that the amount of power to the load is increased gradually. It continues until the load current value reaches the threshold value **32**. Then the error amplifier **30** takes over the control of PIN **4** which is the charge on the capacitor, as described herein. For CCFL loads, it is known that a gradual increase in lamp current helps to ensure the life of the lamp.

Thus, PIN **4** is adapted to generate the DC signal CMP **52** based on the values of the error signal generated by the current control circuit **300** and/or the dimming signal generated by the dimming circuit **200**. PIN **4** is multifunctional since it is also adapted to generate a soft start signal **52** based on the value of the error signal generated by the current control circuit **300**.

FIG. **5** depicts representative signal graphs for certain signals generated by the controller **10** of the present invention. FIG. **5**A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **5**D. FIG. **5**B depicts the burst mode signal (LPWM) **50**, and FIG. **5**C depicts the load current I_L. When the burst mode signal is deasserted (high) **50**A, the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50**B, the drive signals stop and the lamp current is approximately zero. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (approximately zero) as described above.

FIG. **2** depicts another exemplary inverter controller **10'** according to the present invention. The inverter controller **10'** of this exemplary embodiment operates in a similar manner as described above with reference to FIG. **1**, but includes additional circuitry which may be desirable for a given operating environment. For example, at the output of error amplifier **30** is an on/off circuit triggered by the OVP signal. If the overvoltage protection circuit is activated, the OVP signal shuts the output of the error amplifier **30** off, regardless of the value of Isens. Thus, when the OVP signal is asserted, block **30** neither sources no sinks capacitor **40**. Of course, the protection circuitry may also be adapted to charge or discharge the capacitor **40** to some minimum level so that the output signals deliver a predetermined minimum pulse width to the load during the time out period.

The controller **10'** also includes a min/max circuit **56** which, during times when the burst mode signal is enabled, generates a minimum DC value (instead of a zero DC value **52**, as described above during these periods). Thus, the intersection between the sawtooth signal and the minimum DC signal generated by the min/max circuit **56** generates an output to cause the output signals to have some predetermined minimum pulse width. This prevents, for example, wide voltage swings and/or maintains continuous function of the drive signals between burst mode signal asserted and burst mode signal deasserted.

An enable comparator **58** is provided to generate an enable control signal to the switch logic **44**. The comparator generates an enable signal (thereby enabling the switch logic) if the value on the capacitor **40** is greater than the enable threshold value or else the switch logic is disabled.

The PWM enable circuit **38'** may include a floor value (i.e., bias), below which the PWM enable circuit will not sink charge from the CMP capacitor **40**. Like the min/max circuit, this prevents the burst mode enabled signal from completely sinking the charge on the capacitor, so that the output signals are set at a predetermined minimum other than zero. The value of the bias may be selected in accordance with the operating range of the controller, a desired minimum power delivered to the load during burst mode assertion, and/or other factors that will be apparent to those skilled in the art.

FIG. **6** depicts representative signal graphs for certain signals generated by the controller **10'** of the present invention. FIG. **6**A shows the drive signals NDR1 and NDR2. The pulse width of the drive signals is determined by the intersection of the DC error signal CMP **52** and the sawtooth signal CT, as depicted in FIG. **6**D. FIG. **6**B depicts the burst mode signal (LPWM) **50'**, and FIG. **6**C depicts the load current I_L. When the burst mode signal is deasserted (high) **50**A', the drive signals and lamp current are present. When the burst mode signal is asserted (low) **50**B', the drive signals are reduced to a predetermined minimum pulse

width and the lamp current is significantly reduced. The asserted value of the burst mode signal **50B'** is biased in a manner described above. Note that when the burst mode signal is asserted the CMP signal drops to a minimum value (greater than zero), as described above.

Thus, the exemplary inverter controller ICs **10** and **10'** of FIGS. **1** and **2** include a pin (e.g., PIN**2**) that is multiplexed to receive a first input signal (e.g., Vdim or Vsens) with a first predefined range, and a second signal with a second predefined range. The inverter controller ICs **10** and **10'** are also adapted to include a pin (e.g., PIN **4**) that is multifunctional to operate in a first time period (e.g., normal operating conditions) and a second time period (e.g., initial power using soft start loading).

FIG. **3** depicts an exemplary application topology for the inverter controller IC **10** or **10'**. The controller IC **10** or **10'** depicted in FIG. **3** is used to drive a derived Royer circuit comprised of transistors Q1 and Q2, to power a CCFL load **66**. Q1 and Q2 drive the primary side of the transformer **60**, through a resonant tank circuit formed by the capacitor **68** and the primary side inductance of the transformer **60**. The operation of this type of circuit is well known by those skilled in the art. Vsen is derived from a voltage divider between capacitors C1 and C2 (node **62**) so that the value of Vsen is nominal compared to the voltage at the secondary side of the transformer. Vsen is typically in the range of 1 to 5 Volts. Isen is derived from the CCFL load through the divider circuit of R1 and R2 (node **64**). Isen will typically range between 0 Volts (no lamp) to 1.25 Volts (full lamp brightness). Of course, these values are only exemplary, and may be modified to meet design criteria without departing from the present invention. FIG. **4** represents another exemplary application topology for the inverter controller **10** or **10'**. The controller in this embodiment is used to drive two (or more) CCFL loads **66** and **70**.

Those skilled in the art will recognize numerous modifications that may be made to the present invention. For example, the controller ICs **10** and **10'** of FIGS. **1** and **2** multiplex the values of Vsen and DIM on PIN **2**, and combine the functionality of the charge capacitor CMP **40** and soft start functionality. However, these are only examples of pin multiplexing/multitasking that may be accomplished by the present invention. Other pins associated with the exemplary IC may be multiplexed and/or multitasked. Additionally, other IC designs that require more or fewer pins than the 8 pin IC depicted in FIGS. **1** and **2** may likewise include pin multitasking and/or multiplexing as provided herein.

Still other modifications may be made. In the exemplary controller ICs of FIGS. **1** and **2**, PIN **2** is multiplexed to support both load voltage sensing and dim signal input. The range of dim signals (V1<Vdim<V2), as disclosed above, and the overvoltage protection threshold Vovp are selected such that Vovp>V2. However, this relationship is not required for the present invention to operate properly. Indeed Vovp may be selected within or below the range of Vdim, since the Vdim value is used by the overvoltage protection circuit **100**, independent of the dim value. Alternatively, the multiplexed and/or multifunctional pins disclosed herein may be adapted to support three or more signals, using multiplexing and or multifunctional techniques provided herein.

Still other modifications may be made. For example, the exemplary application topologies of FIGS. **3** and **4** depict the controller ICs **10** or **10'** driving a derived Royer circuit formed by Q1 and Q2. However, the controller **10** or **10'** may be likewise applied to a push-pull inverter, a half bridge inverter and/or other type of two switch inverter topology known in the art. Yet further, the controller IC **10** or **10'** may be modified to include a second pair of drive signals (e.g., PDR1 and PDR2) to enable the controller IC **10** or **10'** to drive a four switch inverter topology (e.g., full bridge inverter).

The present invention is not limited to a CCFL load. Indeed the controller **10** or **10'** of the present invention may be used to drive other lamp loads, such as metal halide or sodium vapor. Still other loads may be used. For example, the controller **10** or **10'** of the present invention may be adapted to operate in a frequency range to support driving an x-ray tube or other higher frequency load. The present invention is not limited to the load type, and should be construed as load independent. Additionally, for multiple lamp topologies such as depicted in FIG. **4**, numerous other topologies may be used, for example as described in U.S. Pat. No. 6,104,146, and U.S. patent application Ser. Nos. 09/873,669, 09/850,692, and 10/035,973, all of which are incorporated by reference in their entirety.

A detailed discussion of the operation of certain components of FIGS. **1** and **2** has been omitted. For example, the operation of the oscillator circuit **12** and the operation of the switch logic **44** have been omitted since it is assumed that one skilled in the art will readily recognize both the operation and implementation of these features. Also, the timing of the drive signals NDR1 and NDR2 is not described at length herein, since the operation of these signals will be apparent to those skilled in the art. The preceding detailed description of the block diagrams of FIGS. **1** and **2** is largely directed to the functionality of the components. The components of FIGS. **1** and **2** may be off-the-shelf or custom components to achieve the functionality stated herein, and those skilled in the art will readily recognize that many circuit implementations may be used to accomplish the functionality stated herein, and all such alternatives are deemed within the scope of the present invention.

Still further, inverter controller circuits that include voltage and current feedback, and dimming control (as described herein) are well known to those skilled in the art. However, the prior art integrated circuit inverter controllers have failed to address the long-felt need to reduce the IC package pin count while maintaining the functionality of the inverter IC. The present invention described herein provides examples of addressing this issue by providing, for example, multiplexed and/or multifunctional IC pins. Numerous modifications to this inventive theme will be apparent to those skilled in the art, and all such modifications are deemed within the scope of the present invention, as set forth in the claims.

The invention claimed is:

1. An inverter controller integrated circuit (IC) for generating power to a load, comprising:

an overvoltage protection circuit configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load;

a dimming circuit configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load;

a current control circuit configured to receive a current feedback signal from the load and configured to generate an error signal; and

an output circuit configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load;

wherein said IC further comprises a pin configured to receive said voltage feedback signal and said dimming

signal, wherein said voltage feedback signal and said dimming signal each comprise independent signals that are used by said IC during operation of said IC, and wherein said IC further comprises a multiplexer coupled to said pin and configured to direct said voltage feedback signal to said overvoltage protection circuit or said dimming signal to said dimming circuit, based on the value of said current feedback signal.

2. An inverter controller IC as claimed in claim **1**, wherein said current control circuit comprising a first comparator configured to compare said current feedback signal to a load threshold signal indicative of a minimum current that should be present at the load, said comparator configured to generate a control signal for controlling the state of said multiplexer.

3. An inverter controller IC, comprising:

an overvoltage protection circuit configured to receive a voltage feedback signal from the load and configured to generate a protection signal to discontinue power to the load;

a dimming circuit configured to receive a dimming signal and configured to generate a dimming signal to control the power delivered to the load;

a current control circuit configured to receive a current feedback signal from the load and configured to generate an error signal; and

an output circuit configured to receive said error signal and said dimming signal and configured to generate drive signals for driving said load;

wherein said IC further comprises a pin configured to receive said error signal and said dimming signal, and adapted to generate a first signal based on the values of the error signal and/or the dimming signal or second signal based on the value of the error signal, and wherein said error signal and said dimming signal each comprise independent signals that are used by said IC during operation of said IC.

4. An integrated circuit, comprising an inverter controller comprising an input pin configured to receive two or more independent input signals, each said independent signal supporting an associated function of said controller; wherein one of said independent input signals is present in a first time period and another of said independent input signals is present in a second time period, and wherein each said independent signal supporting an associated function of said controller during operation of said controller.

5. An integrated circuit, comprising an inverter controller comprising a multiplexer and a plurality of input pins; wherein at least one of said input pins configured to receive two or more independent input signals, each said independent signal being multiplexed to support an associated function of said controller each said independent signal supporting an associated function of said controller during operation of said controller.

6. An IC as claimed in claim **5**, wherein said input pin configured to receive a first signal representing a dim voltage, said first signal having a first voltage range; and a second signal representing a voltage feedback signal, said second signal having a second voltage range.

7. An IC as claimed in claim **5**, wherein said multiplexer directs one of said input signals to a first circuit to support a first said function of said controller, and said multiplexer directs another of said input signals to a second circuit to support a second said function of said controller.

8. An IC as claimed in claim **5**, further comprising another input pin configured to receive two or more input signals, each said signal supporting an associated function of said controller; wherein one of said input signals is present in a first time period and another of said input signals is present in a second time period.

9. An IC as claimed in claim **8**, wherein the input pin is configured to receive the first signal representing a current feedback signal, where the first signal is present in a first time period; and a second signal representing a soft start signal, where the second signal is present in the second time period.

10. An IC as claimed in claim **5**, wherein the input pin is configured to receive a first signal representing a current feedback signal, where the first signal is present in a first time period; and a second signal representing a soft start signal, where the second signal is present in a second time period.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,120,035 B2
APPLICATION NO. : 10/690103
DATED : October 10, 2006
INVENTOR(S) : Lin et al.

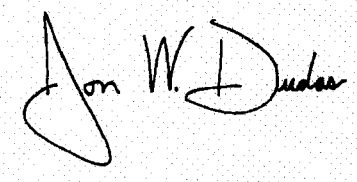
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 10, line 30, in Claim 9, delete "the" and insert -- a --, therefor.

In column 10, line 31, in Claim 9, after "in" delete "a" and insert -- the --, therefor.

Signed and Sealed this

Twenty-sixth Day of December, 2006



JON W. DUDAS
Director of the United States Patent and Trademark Office

Exhibit 11

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Int'l Trade Commission

December 15, 2008

CBI 09-83

HAND DELIVERY

The Honorable Marilyn R. Abbott
Secretary
U.S. International Trade Commission
500 E Street, S.W.
Washington, DC 20436

RECEIVED
OFFICE OF THE SECRETARY
U.S. INTERNATIONAL TRADE COMM
2008 DEC 15 PM 4:01

Re: Certain Cold Cathode Fluorescent Lamp ("CCFL") Inverter Circuits and Products Containing Same

Dear Secretary Abbott:

Enclosed for filing on behalf of O2 Micro International Ltd. and O2 Micro Inc. ("collectively O2 Micro") are the following documents in support of O2 Micro's request that the Commission commence an investigation pursuant to section 337 of the Tariff Act of 1930, as amended. Pursuant to the Commission Rules of Practice and Procedure, a request for confidential treatment of Confidential Exhibits 34-48 is concurrently being transmitted with this filing. O2 Micro submits the following:

1. an original and twelve (12) copies of O2 Micro's verified Complaint (Rule 210.8 (a));

2. an original and six (6) copies of the exhibits to the Complaint with the confidential exhibits 34-48 segregated from the non-confidential exhibits (original plus one copy unbound, without tabs (Rules 201.6(c), 210.4(f)(3)(i) and 210.8(a));

3. ten (10) additional copies of the Complaint and accompanying exhibits, both confidential and non-confidential, for service upon the proposed respondents Monolithic Power Systems Inc., Microsemi Corporation, ASUSTeK Computer Inc., ASUSTeK Computer International America, LG Electronics, LG Electronics U.S.A., LG Display Co., Ltd., LG Display America, Inc., BenQ Corporation and BenQ America Corp. and two (2) additional copies of the verified Complaint and accompanying non-confidential exhibits for service upon the Taipei Economic and Cultural Representative Office and the Embassy of the Republic of Korea (Rules 210.4(f)(3)(i), 210.8(a) and 210.11(a));

4. certified copies of U.S. Patent Nos. 7,417,382 ("the '382 patent"), 6,856,519 ("the '519 patent"), 6,809,938 ("the '938 patent") and 7,120,035 ("the '035 patent") (legible copies of the patents are included in the Complaint as Exhibits 1-4 (Rule 210.12(a)(9)(i)));

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December 15, 2008

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HAND DELIVERY

The Honorable Marilyn R. Abbott
Secretary
U.S. International Trade Commission
500 E Street, S.W.
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Re: Certain Cold Cathode Fluorescent Lamp ("CCFL") Inverter Circuits and Products Containing Same

Dear Secretary Abbott:

I am counsel for Complainants O2 Micro International Ltd. and O2 Micro Inc. ("collectively O2 Micro"). In accordance with Commission Rules 201.6 and 210.5, O2 Micro requests confidential treatment of business information contained in Confidential Exhibits 34-48 to the Complaint.

The information for which confidential treatment is sought is proprietary commercial and technical information not otherwise publicly available. Specifically, the exhibits contain the following:

Confidential Exhibit 34: O2 Micro's Licensees, the identity and content of which are proprietary business information that is not publicly available;

Confidential Exhibit 35: Claim Chart demonstrating practice of claim 1 of '382 patent by CCFL inverter circuit with OZ960, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 36: Claim Chart demonstrating practice of claim 1 of '382 patent by CCFL inverter circuit with OZ964, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 37: Claim Chart demonstrating practice of claim 1 of '519 patent by CCFL inverter circuit with OZ9RRA, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 38: Claim Chart demonstrating practice of claim 1 of '519 patent by CCFL inverter circuit with OZ9936, which contains proprietary technical information that is not publicly available;

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5. certified copies of the assignments for the '382, '519, '938 and '035 patents (legible copies of the assignments for the '382, '519, '938 and '035 patents are included in the Complaint as Exhibits 5-7 (Rule 210.12(a)(9)(ii)));

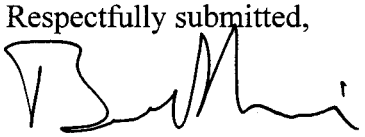
6. certified copies and three (3) additional copies (on CD) of the prosecution histories for the '382, '519, '938 and '035 patents (bearing bates nos. O2ITC 000001 - O2ITC 015794, O2ITC 034047-O2ITC 034480, O2ITC 036665-O2ITC 036740 and O2ITC 036791-O2ITC 037069) (Rule 210.12(c)(1));

7. four (4) copies (on CD) of each technical reference document mentioned in the prosecution histories of the '382, '519, '938 and '035 patents (bearing bates nos. O2ITC 015795 - O2ITC 034046, O2ITC 034481-O2ITC 036664, 036741-O2ITC 036790 and O2ITC 037070-O2ITC 037230) (Rule 210.12(c)(2)); and

8. a letter and certification pursuant to Commission Rules 201.6(b) and 210.5(d) requesting confidential treatment of Confidential Exhibits 34-48.

Thank you for your attention to this matter.

Respectfully submitted,



Bert C. Reiser
Counsel for Complainants
O2 Micro International Ltd. and
O2 Micro Inc.

Enclosures

Confidential Exhibit 39: Claim Chart demonstrating practice of claim 1 of '938 patent by CCFL inverter circuit with OZ9RRA, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 40: Claim Chart demonstrating practice of claim 1 of '938 patent by CCFL inverter circuit with OZ9936, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 41: Claim Chart demonstrating practice of claim 4 of '035 patent by CCFL inverter circuit with OZ9RRA, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 42: Claim Chart demonstrating practice of claim 4 of '035 patent by CCFL inverter circuit with OZ9936, which contains proprietary technical information that is not publicly available;

Confidential Exhibit 43: Total Volume and Revenue from OZ960, OZ964, OZ9RRA and OZ9936, which contains proprietary business information that is not publicly available;

Confidential Exhibit 44: Wafer Supply Agreement, which contains proprietary business and technical information that is not publicly available;

Confidential Exhibit 45: O2 Micro's Investment in its U.S. Facility Where Designing, Developing, Testing and Support for OZ960, OZ964, OZ9RRA and OZ9936 Occurs, containing proprietary business information that is not publicly available;

Confidential Exhibit 46: O2 Micro's Approximate Dollar Investment in Designing, Developing, Testing and Support for OZ960, OZ964, OZ9RRA and OZ9936, containing proprietary business information that is not publicly available;

Confidential Exhibit 47: O2 Micro's Expenditures in Fabrication Facility where OZ964, OZ9RRA and OZ9936 are Fabricated, containing proprietary business information that is not publicly available; and

Confidential Exhibit 48: O2 Micro's Employees Engaged In Designing, Developing, Testing and Support for OZ960, OZ964, OZ9RRA and OZ9936, which contains proprietary business information that is not publicly available.

The information described above qualifies as confidential business information pursuant to Rule 201.6(a) in that:

a) it is not available to the public;

b) unauthorized disclosure of such information could cause substantial harm to the competitive position of Complainant O2 Micro; and

HOWREY LLP

c) the disclosure of which could impair the Commission's ability to obtain information necessary to perform its statutory function.

Respectfully submitted,

Bert C. Reiser
Counsel for Complainants
O2 Micro International Ltd. and
O2 Micro Inc.

SUBSCRIBED AND SWORN before me the 15th day of December, 2008

Notary Public

Olga A. Bunzik
Notary Public, District of Columbia
My Commission Expires 8-14-2010

UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.

In the Matter of CERTAIN COLD CATHODE FLUORESCENT LAMP ("CCFL") INVERTER CIRCUITS AND PRODUCTS CONTAINING SAME	Investigation No. 337-TA-___

COMPLAINT UNDER SECTION 337 OF
THE TARIFF ACT OF 1930, AS AMENDED

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3. U.S. Patent No. 6,809,938
4. U. S. Patent No. 7,120,035
5. Assignment for '382 patent
6. Assignment for '519 patent
7. Assignments for '938 and '035 patents
8. Form 10-K/A Monolithic Power Systems Inc., filed May 12, 2008
9. MPS Company Information from http://www.monolithicpower.com/cmp_01_info.htm, dated September 19, 2008
10. Backlight – CCFL Drivers Parametric Table from http://products.monolithicpower.com/Products/ParametricTable.do?categoryId=17, dated September 19, 2008
11. Form 10-K Microsemi Corporation for the fiscal year ended September 30, 2007
12. Company Profile from http://www.microsemi.com/aboutus.asp, dated September 5, 2008
13. products: CCFL Backlight Controller IC, from http://www.microsemi.com/catelog/parmlist.asp?P0_CAT=PM&P1_TYPE=BLIC&LVP=1&LVP1=0, dated September 5, 2008
14. Photographs of the ASUSTeK F5RL-B2 notebook PC containing an inverter circuit with MPS MP1010BEP
15. Photographs of the LG 32LB9D 32" LCD television containing an inverter circuit with Microsemi LX1691
16. LGE US Division from http://us.lge.com/about/company/lge_us.jsp, dated September 25, 2008
17. Form 20-F LG Display Co., Ltd. filed April 16, 2008
18. BenQ Group from http://benq.com/page/?pageId--477, dated November 14, 2008
19. Products from http://www.benq.us/products/, dated November 18, 2008

20. Offer for Sale of E2200HD from http://store.benq.us/benq-us/searchresults.aspx?keyword=E2200HD&culture+en-US, dated November 18, 2008

21. Photographs of the BenQ E2200HD Series LCD Monitor containing an inverter circuit with MPS MP1009

22. Claim Chart showing infringement of independent claims 1 and 8 of the '382 Patent by ASUS F5RL-B2 notebook PC with the MP1010B

    A. Photographs of ASUSTeK F5RL-B2 notebook PC

    B. MP1010B Datasheet

    C. Schematic of inverter circuit with MP1010B in ASUSTeK F5RL-B2

    D. Test results from inverter circuit with MP1010B in ASUSTeK F5RL-B2

23. Claim Chart showing infringement of independent claims 1 and 8 of the '382 Patent by LG 32BL9D 32" LCD television with LX1691

    A. Photographs of Model 32LB9D television with LX1691

    B. LX1691 Datasheet

    C. Schematic of inverter circuit with LX1691 in LG 32LB9D

    D. Test results from inverter circuit with LX1691 in LG 32LB9D

24. Claim Chart showing infringement of claim 7 of the '519 patent by BenQ E2200HD LCD monitor with the MP1009 inverter circuit

25. Claim Chart showing infringement of independent claim 1 of the '938 patent by BenQ E2200HD LCD monitor with inverter circuit with MP1009

26. Claim Chart showing infringement of claim 4 of the '035 patent by BenQ E2200HD LCD monitor with inverter circuit with MP1009

27. Photographs of the BenQ E2200HD LCD monitor with MP1009

28. Schematic of the inverter circuit with MP1009 in BenQ E2200HD

29. Test results from inverter circuit with MP1009 in BenQ E2200HD

30. Complaint for Declaratory Judgment

31. Receipt reflecting purchase of ASUS F5RL-B2 notebook PC

32. Receipt reflecting purchase of LG 32BL9D 32" LCD television

33. Receipt reflecting purchase of BenQ E2200HD LCD monitor

34. **CONFIDENTIAL:** O2 Micro's Licensees

35. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '382 patent by CCFL inverter circuit with OZ960.

    A. **CONFIDENTIAL:** OZ960 Datasheet

36. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '382 patent by CCFL inverter circuit with OZ964.

    A. **CONFIDENTIAL:** OZ964 Datasheet

    B. **CONFIDENTIAL:** OZ964 Preliminary Datasheet

37. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '519 patent by CCFL inverter circuit with OZ9RRA.

    A. **CONFIDENTIAL:** OZ9RRA Datasheet

38. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '519 patent by CCFL inverter circuit with OZ9936.

    A. **CONFIDENTIAL:** OZ9936 Datasheet

39. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '938 patent by CCFL inverter circuit with OZ9RRA.

    A. **CONFIDENTIAL:** OZ9RRA Datasheet

40. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 1 of '938 patent by CCFL inverter circuit with OZ9936.

    A. **CONFIDENTIAL:** OZ9936 Datasheet

41. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 4 of '035 patent by CCFL inverter circuit with OZ9RRA

    A. **CONFIDENTIAL:** OZ9RRA Datasheet

42. **CONFIDENTIAL:** Claim Chart demonstrating practice of claim 4 of '035 patent by CCFL inverter circuit with OZ9936

    A. **CONFIDENTIAL:** OZ9936 Datasheet

43. **CONFIDENTIAL:** Total Volume and Revenue from OZ960, OZ964, OZ9RRA and OZ9936

44. **CONFIDENTIAL:** Wafer Supply Agreement

I. INTRODUCTION

1.1 Complainants O2 Micro International Ltd. and O2 Micro Inc. (collectively hereinafter "O2 Micro" or "Complainants") request the U.S. International Trade Commission ("ITC") to commence an investigation pursuant to section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337(a)(1)(B)(i) ("section 337"), and to remedy the unlawful importation into the United States, the sale for importation, and/or the sale within the United States after importation by the owner, importer, or consignee, of articles covered by valid and enforceable United States patents owned by O2 Micro International Ltd.

1.2 The proposed respondents, Monolithic Power Systems Inc. ("MPS"), Microsemi Corporation ("Microsemi"), ASUSTeK Computer Inc., ASUSTeK Computer International America (collectively "ASUSTeK"), LG Electronics, LG Electronics U.S.A., LG Display Co, Ltd., LG Display America, Inc. (collectively "LG"), BenQ Corporation and BenQ America Corp. (collectively "BenQ") (all collectively "Respondents"), have engaged in unfair acts in violation of section 337 through the unlicensed importation, sale for importation and/or sale after importation of certain cold cathode fluorescent lamp ("CCFL") inverter circuits with MPS or Microsemi inverter controllers and products containing the same covered by one or more claims of Complainants' U.S. Patent Nos. 7,417,382 ("the '382 patent"), 6,856,519 ("the '519 patent"), 6,809,938 ("the '938 patent"), and 7,120,035 ("the '035 patent").

1.3 Certified copies of the '382, '519, '938 and '035 patents accompany this complaint as **Exhibits 1, 2, 3, and 4**. O2 Micro International Ltd. owns by assignment the entire right, title and interest in and to these patents. Certified copies of the recorded assignments of these patents accompany this complaint as **Exhibit 5, 6, and 7.**

1.4 As required by section 337(a)(2) and defined by section 337(a)(3), an industry exists in the United States relating to certain CCFL inverter circuits and products containing the same protected by the asserted patents. The domestic industry for the asserted patents includes O2 Micro's substantial United States investments and expenditures in activities, including the designing, developing, manufacturing, testing and support, of CCFL inverter circuits that utilize and exploit the inventions claimed in the asserted patents.

1.5 O2 Micro seeks exclusion orders pursuant to section 337(d) excluding from entry into the United States Respondents' CCFL inverter circuits and products containing Respondents' infringing CCFL inverter circuits covered by one or more claims of the asserted patents. O2 Micro further seeks cease and desist orders directed to Respondents to halt the importation, marketing, advertising, demonstration, warehousing of inventory for distribution, sale and use of such imported products in the United States pursuant to section 337(f).

II. COMPLAINANTS

2.1 Complainant O2 Micro International Ltd. is a corporation organized under the laws of the Cayman Islands with its principal place of business at The Grand Pavilion, West Bay Road, PO Box 32331 SMB, George Town, Grand Cayman, Cayman Islands. O2 Micro International Ltd. designs, develops and markets high performance integrated circuits for power management and security operations, as well as systems security solutions. O2 Micro's 2007 Annual Report is available on O2 Micro's website at: http://phx.corporate-ir.net/phoenix.zhtml?c=123458&p=irol-reportsannual.

2.2 Complainant O2 Micro Inc. is a wholly owned subsidiary of O2 Micro International Ltd. located at 3118 Patrick Henry Drive, Santa Clara California. O2 Micro Inc.

designs, develops, tests, sells and supports O2 Micro's products, including its family of CCFL inverter controllers for its inverter circuit designs.

2.3 In introducing its CCFL inverter controllers for its inverter circuit designs, O2 Micro revolutionized the way to safely and efficiently control power in backlighting for liquid crystal displays ("LCDs"). Since that time, O2 Micro's innovations for controlling power to LCD backlighting have become widely accepted by leading notebook computer, LCD TV and LCD monitor companies. O2 Micro continues to invest millions of dollars in research and development of not only new products, but also in existing products, such as its CCFL inverter controllers for inverter circuits, to maintain its competitiveness. This development activity occurs primarily in the United States.

2.4 O2 Micro has sought and obtained patent protection in the United States for a number of inventions relating to CCFL inverter circuits, including the inventions claimed in the '382, '519, '938 and '035 patents.

III. PROPOSED RESPONDENTS

3.1 Respondent Monolithic Power Systems Inc. ("MPS") is a Delaware corporation with its corporate headquarters located at 6409 Guadalupe Mines Road, San Jose, California. Upon information and belief, MPS manufactures, markets, sells for importation, imports and/or sells after importation into the United States analog and mixed-signal semiconductors, including those for infringing CCFL inverter circuits. *See* **Exhibit 8 at 28.** Upon further information and belief, MPS manufactures its infringing CCFL inverter controllers for inverter circuits overseas and sells these infringing CCFL inverter controllers for inverter circuits to original equipment manufacturers for importation into the United States in various products, including notebook

computers, LCD televisions and LCD displays. *See* **Exhibit 8 at 7, 10 and Exhibit 9.** Examples of these infringing CCFL inverter controllers for inverter circuits include, but are not limited to, the following MPS product families MP1009, MP1010B, MP1026, MP1038, and MP1048. *See* **Exhibit 10.**

3.2 Respondent Microsemi Corporation ("Microsemi") is a Delaware corporation located at 2381 Morse Avenue, Irvine, California. Upon information and belief, Microsemi manufactures, markets, sells for importation, imports and/or sells after importation into the United States analog and mixed-signal integrated circuits and semiconductors, including infringing CCFL inverter controllers for inverter circuits. *See* **Exhibits 11 at 6, 52 and Exhibit 12.** Upon further information and belief, Microsemi sells its infringing CCFL inverter controllers for inverter circuits to original equipment manufacturers for importation into the United States in various products, including notebook computers, LCD televisions and LCD displays. *See* **Exhibit 11 at 6.** Examples of Microsemi's infringing CCFL inverter controllers for inverter circuits include, but are not limited to, the following product families: LX1686; LX1688; LX1689; LX1691; LX1692; LX1692A; LX 1693; LX1695; LX1696; LX1697; LX6501; and LX6512. *See* **Exhibit 13.**

3.3 Respondent ASUSTeK Computer Inc. is a Taiwanese corporation located at No. 15, Li-Te Road, Peitou, Taipei, Taiwan. Upon information and belief, ASUSTeK Inc. manufactures, sells for importation, imports and/or sells after importation into the United States notebook computers and/or LCD monitors that contain infringing CCFL inverter circuits with MPS inverter controllers. An example of such a product is the F5RL-B2 notebook computer. *See* **Exhibit 14.**

3.4 Respondent ASUSTeK Computer International America is located at 800 Corporate Way, Fremont California. ASUSTeK Computer International America is a wholly owned subsidiary of ASUSTeK Computer Inc. Upon information and belief, ASUSTeK Computer International America sells for importation, imports and/or sells after importation into the United States notebook computers and/or LCD monitors that contain infringing CCFL inverter circuits with MPS inverter controllers.

3.5 Respondent LG Electronics ("LG") is a Korean corporation located at LG Twin Towers 20, Yoido-dong, Youngdungpo-gu, Seoul, Korea. Upon information and belief, LG manufactures, sells for importation, imports and/or sells after importation into the United States notebook computers and/or LCD televisions that contain infringing CCFL inverter circuits with Microsemi inverter controllers. An example of such a product is the 32LB9D LCD television. *See* **Exhibit 15.**

3.6 Respondent LG Electronics U.S.A. is a Delaware corporation and a wholly owned subsidiary of LG Electronics whose office is located at 1000 Sylvan Avenue, Englewood Cliffs, New Jersey. Upon information and belief LG Electronics U.S.A. markets, imports and/or sells after importation in the United States the notebook computers and/or LCD televisions that contain infringing CCFL inverter circuits manufactured and designed by LG Electronics. *See* **Exhibits 15 and 16.**

3.7 Respondent LG Display Co., Ltd. ("LG Display") is a Korean corporation located at West Tower, LG Twin Towers, 20, Yoido-dong, Youngdungpo-gu, Seoul, Korea. Upon information and belief, LG Display designs, manufactures, sells for importation, imports and/or sells after importation into the United States LCD panels that contain infringing CCFL inverter circuits, primarily for use in televisions, notebook computers and desktop monitors. *See*

Exhibit 17 at 26, 32. LG Display is a subsidiary of LG Electronics. *Id.* Further upon information and belief, LG Display manufactures its LCD panels outside of the United States in Korea, Poland and China. **Exhibit 17 at 27**.

3.8 Respondent LG Display America, Inc. ("LG Display America") is a California corporation located at 150 East Brokaw Road, San Jose, CA 95112. LG Display America is a wholly owned subsidiary of LG Display. **Exhibit 17 at 42**. Upon information and belief, LG Display America sells for importation, imports and/or sells after importation into the United States TFT-LCD panels with infringing CCFL inverter circuits. **Exhibit 17 at 36.**

3.9 Respondent BenQ Corporation is a Taiwanese corporation located at 16 Jihu Road, Neihu, Taipei 114, Taiwan. Upon information and belief, BenQ manufactures, sells for importation, imports and/or sells after importation into the United States notebook computers, LCD displays and/or LCD panel televisions that contain infringing MPS CCFL inverter circuits. *See* **Exhibit 18.** An example of such a product is the E2200HD Series LCD Monitor containing the MP1009. *See* **Exhibit 19.**

3.10 Respondent BenQ America Corp. is a California corporation and a wholly owned subsidiary of BenQ Corporation whose office is located at 15375 Barranca, Suite A205, Irvine, California. Upon information and belief BenQ America Corp. markets, imports and/or sells after importation in the United States the notebook computers, LCD displays and/or LCD panel televisions that contain infringing CCFL inverter circuits. *See* **Exhibits 20 and 21.**

3.11 Upon information and belief, MPS and Microsemi sell their CCFL inverter controllers for inverter circuits directly or indirectly to their customers overseas, such as AUSTeK, LG Display, LG and BenQ. These CCFL inverter circuits are then placed into

products, such as LCD panels, notebook computers, LCD televisions and/or LCD monitors, which are sold for importation, imported and/or sold after importation into the United States by numerous companies including BenQ, LG and ASUSTeK.

IV. THE PRODUCTS AT ISSUE

4.1 The products at issue in this investigation are certain CCFL inverter circuits and products containing the same.

4.2 A notebook computer screen or other LCD display requires a white light behind it to display all the colors. This white light is generated by one or more fluorescent tubes, which, unlike regular fluorescent tubes, do not generate much heat and are therefore known as cold cathode fluorescent lamps, or CCFLs. These CCFLs require up to 1200 volts or more of alternating current (AC) to light up (depending upon the geometry of the CCFLs). Changing voltage from a direct current (DC) battery to about 1200 volts or more AC requires a circuit named an inverter. An inverter controller circuit is also known as a DC-to-AC converter circuit. The high voltage delivered by the inverter circuit excites gas inside the lamp, and the energized ions absorbed by the phosphor coating on the lamp emit light.

4.3 O2 Micro designs and develops CCFL inverter circuits that are used in computer notebooks, televisions and LCD monitors. Examples from O2Micro's family of CCFL inverter circuits include the OZ960, OZ964, OZ9RRA, and OZ9936.

4.4 Upon information and belief, Respondents sell for importation, import, and sell after importation certain CCFL inverter circuits and products containing the same that infringe the asserted patents.

V. THE PATENT-IN-SUIT

A. The '382 Patent

1. Identification of the Patent and Ownership by O2 Micro

5.1 U.S. Patent No. 7,417,382 ("the '382 patent") (**Exhibit 1**), entitled "High-Efficiency Adaptive DC/AC Converter," was issued on August 26, 2008. O2 Micro International Ltd. is the assignee (*see* **Exhibit 5**) and Yung-Lin Lin is named as the sole inventor.

5.2 Pursuant to Rule 210.12(c) of the Commission's Rules of Practice and Procedure, this Complaint is accompanied by the following: (1) a certified copy and three additional copies of the prosecution history of the '382 patent (bearing bates nos. O2ITC 000001 - O2ITC 015794); and (2) four copies of each reference document mentioned in the prosecution history (bearing bates nos. O2ITC 015795 - O2ITC 034046).

2. Non-Technical Description of the Patented Invention

5.3 The '382 patent involves technology for safely providing power to light liquid crystal displays (LCDs) in notebook computers, computer monitors, LCD TVs, portable DVD players, and other consumer electronic products.

5.4 The '382 patent provides an improved inverter circuit for controllably delivering power to CCFLs. An inverter circuit receives DC, but CCFLs only work with AC. DC is converted to AC by turning one or more pairs of switches on and off. The switches are coupled to a transformer. When the on-time of two switches (or sets of switches) overlaps, voltage is applied to the transformer. The transformer creates a magnetic field with a pair of wire windings: one winding defines the primary side of the transformer and the other defines the secondary side of the transformer. Due to the characteristics of the windings, when a certain voltage (for example 12V or 20V) is applied to the primary side, a much higher voltage (at times

exceeding 1,000V) exits the secondary side. Because the voltage is stepped up in this manner, the transformer is known as a step-up transformer. The inverter circuit precisely controls the amount of power delivered to the CCFL by selectively turning on and off the switches. The longer that the switches are conducting and thus the transformer is being energized, the more power that is delivered to the CCFL.

5.5 The '382 patent invention also includes protection circuitry. Because a CCFL requires high voltage, a broken or disconnected lamp (known as an "open lamp condition") creates a danger of sparking, equipment damage, or even injury to the user. But in normal use, the voltage also must be high to cause the lamp to light in the first instance (after which the voltage level drops into a normal operating range). As a result, the high voltage during the start-up period could be confused with high voltage resulting from an open lamp condition. To protect the equipment and the user, but allow the CCFL to operate properly in normal conditions, the '382 patent utilizes a capacitor divider to provide a signal representing the voltage across the CCFL. That signal travels down a feedback signal line to a timer circuit, which has a predetermined time-out duration that is triggered when the voltage is above a certain level. If the voltage remains too high after the time-out duration, the protection circuit shuts down the switches and thereby turns off the CCFL.

3. Foreign Counterparts Sharing the '382 Patent Written Description

5.6 The following is a list of the foreign patents and applications sharing the same written description as the '382 patent:

Country	Type	Number	Status
China	Patent Application	01102605.7	Published/Rejected
China	Patent Application	200710000473	Published
China	Patent (Utility Model)	0420001507	Granted but held invalid in Reexamination
Taiwan	Patent	152318	Granted; Reexamination Pending
Japan	Patent Application	2001-8143	Abandoned
Korea	Patent Application	2001-1901	Abandoned

5.7 Complainant certifies that there are no other foreign patents or patent applications sharing the same written description as the '382 patent that have been issued, abandoned, denied or remain pending.

B. The '519 Patent

1. Identification of the Patent and Ownership by O2 Micro

5.8 U.S. Patent No. 6,856,519 ("the '519 patent") (**Exhibit 2**), entitled "Inverter Controller," was issued on February 15, 2005. O2 Micro International Ltd. is the assignee (*see* **Exhibit 6**) and Yung-Lin Lin and Da Liu are named as the inventors.

5.9 Pursuant to Rule 210.12(c) of the Commission's Rules of Practice and Procedure, this Complaint is accompanied by the following: (1) a certified copy and three additional copies of the prosecution history of the '519 patent (bearing bates nos. O2ITC 034047-O2ITC 034480); and (2) four copies of each reference document mentioned in the prosecution history (bearing bates nos. O2ITC 034481-O2ITC 036664).

2. Non-Technical Description of the Patented Invention

5.10 The '519 patent involves technology related to a system that includes an inverter circuit that generates an alternating current (AC) signal to power one or more cold cathode fluorescent (CCFL) lamps. CCFLs are used to illuminate liquid crystal displays in notebook computers, computer monitors, LCD TVs, portable DVD players, and other consumer electronic products.

5.11 The '519 patent provides improvements to the inverter controller that controls the operation of the CCFL inverter circuit by providing for at least one input pin that is configured to receive at least two independent input signals. The independent input signals each support an associated function of the controller during its operation.

5.12 The use of one or more multifunctional pins used for CCFL inverters as taught by the '519 patent may, for example, results in a reduction of the number of pins needed for an inverter controller and correspondingly provides a benefit to inverter circuit manufacture by decreasing pin count and cost, while maintaining the same functionality.

3. Foreign Counterparts Sharing the '519 Patent Written Description

5.13 The following is a list of the foreign patents and applications sharing the same written description as the '519 patent:

Country	Type	Number	Status
China	Patent	03104111.6	Granted
Hong Kong	Patent	HK1062503	Granted
Japan	Patent	3803652	Granted
Japan	Patent Application	2006-88813	Published
Korea	Patent Application	2003-28509	Pending
Taiwan	Patent	I256764	Granted

5.14 Complainant certifies that there are no other foreign patents or patent applications sharing the same written description as the '519 patent that have been issued, abandoned, denied or remain pending.

C. The '938 Patent

1. Identification of the Patent and Ownership by O2 Micro

5.15 U.S. Patent No. 6,809,938 ("the '938 patent") (**Exhibit 3**), entitled "Inverter Controller," was issued on October 26, 2004. O2 Micro International Ltd. is the assignee (*see* **Exhibit 7**) and Yung-Lin Lin and Da Liu are named as the inventors. This patent is a division of Application No. 10/139,169 issued as the '519 patent.

5.16 Pursuant to Rule 210.12(c) of the Commission's Rules of Practice and Procedure, this Complaint is accompanied by the following: (1) a certified copy and three additional copies of the prosecution history of the '938 patent (bearing bates nos. O2ITC 036665-O2ITC 036740); and (2) four copies of each reference document mentioned in the prosecution history (bearing bates nos. O2ITC 036741-O2ITC 036790).

2. Non-Technical Description of the Patented Invention

5.17 The '938 patent involves technology related to an inverter circuit for converting a direct current (DC) signal into a stepped-up alternating current (AC) signal. The inverter circuit includes power switches, a step-up transformer, and an inverter controller that work together to perform the conversion. For example, the power switches are used to convert a DC signal to an AC signal, a step-up transformer is used to step-up or boost the signal, and the inverter controller generates signals used to drive the power switches to power a load.

5.18 The '938 patent provides improvements to the inverter controller associated with the stepped-up transformer by providing for at least one input pin that is configured to receive at least two independent input signals. The independent input signals each support an associated function of the controller during its operation.

5.19 The use of one or more multifunctional pins used for inverters associated with step-up transformers, as taught by the '938 patent, may, for example, result in a reduction of the number of pins needed for an inverter controller and correspondingly provide a benefit to inverter circuit manufacture by decreasing pin count and cost while maintaining the same functionality.

3. Foreign Counterparts Sharing the '938 Patent Written Description

5.20 The following is a list of the foreign patents and applications sharing the same written description as the '938 patent:

Country	Type	Number	Status
China	Patent	03104111.6	Granted
Hong Kong	Patent	HK1062503	Granted
Japan	Patent	3803652	Granted
Japan	Patent Application	2006-88813	Published
Korea	Patent Application	2003-28509	Pending
Taiwan	Patent	I256764	Granted

5.21 Complainant certifies that there are no other foreign patents or patent applications sharing the same written description as the '938 patent that have been issued, abandoned, denied or remain pending.

D. The '035 Patent

1. Identification of the Patent and Ownership by O2 Micro

5.22 U.S. Patent No. 7,120,035 ("the '035 patent") (**Exhibit 4**), entitled "Inverter Controller," was issued on October 10, 2006. O2 Micro International Ltd. is the assignee (*see* **Exhibit 7**) and Yung-Lin Lin and Da Liu are named as the inventors This patent is a division of Application No. 10/139,169 issued as the '519 patent.

5.23 Pursuant to Rule 210.12(c) of the Commission's Rules of Practice and Procedure, this Complaint is accompanied by the following: (1) a certified copy and three additional copies of the prosecution history of the '035 patent (bearing bates nos. O2ITC 036791-O2ITC 037069); and (2) four copies of each reference document mentioned in the prosecution history (bearing bates nos. O2ITC 037070-O2ITC 037230).

2. Non-Technical Description of the Patented Invention

5.24 The '035 patent involves technology related to inverter controller integrated circuits. The '035 patent provides improvements to inverter controllers by providing for at least one input pin that is configured to receive at least two independent input signals.

5.25 The '035 patent further relates to characteristics of the input signals that might be received, including, for example, when the signals are present. The independent input signals each support an associated function of the controller during its operation.

5.26 The use of inverter controller integrated circuits such as those that are the subject of the '035 patent may, for example, results in a reduction of the number of pins needed for an inverter controller and correspondingly provides a benefit to inverter circuit manufacture by decreasing pin count and cost while maintaining the same functionality.

3. Foreign Counterparts Sharing the '035 Patent Written Description

5.27 The following is a list of the foreign patents and applications sharing the same written description as the '035 patent:

Country	Type	Number	Status
China	Patent	03104111.6	Granted
Hong Kong	Patent	HK1062503	Granted
Japan	Patent	3803652	Granted
Japan	Patent Application	2006-88813	Published
Korea	Patent Application	2003-28509	Pending
Taiwan	Patent	I256764	Granted

5.28 Complainant certifies that there are no other foreign patents or patent applications sharing the same written description as the '035 patent that have been issued, abandoned, denied or remain pending.

VI. UNFAIR ACTS OF THE RESPONDENTS

6.1 Upon information and belief, Respondents' CCFL inverter circuits and products containing the same (the "Accused Products") that infringe at least claims 1, 2, 4, 6, 8, 9, 11 and 13 of the '382 patent have been imported, sold for importation and/or sold after importation into the United States by Respondents. In addition, MPS and ASUSTeK accused products also infringe claims 7 and 14 of the '382 patent. Furthermore, MPS and BenQ's accused products infringe claim 7 of the '519 patent, claims 1, 2, 3, and 6 of the '938 patent and claim 4 of the '035 patent.

6.2 Upon information and belief, the Accused Products are imported, sold for importation and/or sold after importation into the United States by Respondents. Respondents' activities constitute acts of direct and contributory infringement, as well as active inducement to infringe, with respect to at least those claims of the asserted patents identified in paragraph 6.1 above. If continued, such activities will further constitute infringing acts, directly, contributorily and as active inducement to infringe. The Accused Products are especially adapted for, and have

no substantial use other than, infringing the asserted patents. They constitute a material part of the patented inventions, and their sale and promotion actively induces infringement of the patent claims at issue by third parties, including end users. Respondents had notice of the asserted patent since at least the filing of this complaint. Additionally, on information and belief, Respondents had actual knowledge of the asserted patents; for example, with respect to the '519, '938, and '035 patents, MPS filed a declaratory judgment action regarding those patents on or about October 2008 (**Exhibit 30**), which required it to have actual notice at the time. On information and belief, Respondents, including MPS, ASUSTeK, and Microsemi have been in patent litigation with O2Micro before regarding patents in the same family as the '382 patent, and monitor patent activity with respect to O2Micro's patent portfolio. Also on information and belief, O2Micro has notified Respondents in the past about its patent portfolio generally as well as about its ongoing efforts to secure new patents.

6.3 Upon information and belief, MPS and Microsemi supply reference designs for inverter circuits that infringe the '382 patent to other parties who are unknown to O2Micro at this time, and their customers substantially follow the reference designs and therefore infringe claims 1, 2, 4, 6, 8, 9, 11 and 13 of the '382 patent. Upon information and belief, inverter circuits that substantially follow the MPS and Microsemi reference designs are imported, sold for importation and/or sold after importation into the United States, the activities of parties using these reference designs constitute acts of direct and contributory infringement, as well as active inducement to infringe, with respect to at least those claims of the asserted patents identified in this paragraph. If continued, such activities will further constitute infringing acts, directly, contributorily and as active inducement to infringe. These inverter circuits are especially adapted for, and have no substantial use other than, infringing the asserted patents. They constitute a material part of the

patented inventions, and their sale and promotion actively induces infringement of the patent claims at issue by third parties, including end users.

6.4 Upon information and belief, MPS supplies reference designs for inverter circuits that infringe the '519, '938 and '035 patents to other parties who are unknown to O2Micro at this time, and MPS customers substantially follow the reference designs and therefore infringe claim 7 of the '519 patent, claims 1, 2, 3, and 6 of the '938 patent and claim 4 of the '035 patent. Upon information and belief, inverter circuits that substantially follow this MPS reference design are imported, sold for importation and/or sold after importation into the United States, the activities of parties using this reference design constitute acts of direct and contributory infringement, as well as active inducement to infringe, with respect to at least those claims of the asserted patents identified in this paragraph. If continued, such activities will further constitute infringing acts, directly, contributorily and as active inducement to infringe. These inverter circuits are especially adapted for, and have no substantial use other than, infringing the asserted patents. They constitute a material part of the patented inventions, and their sale and promotion actively induces infringement of the patent claims at issue by third parties, including end users.

6.5 A claim chart demonstrating how independent claims 1 and 8 of the '382 patent apply to the ASUSTeK F5AL-B2 notebook containing the CCFL inverter circuit with MPS 1010BEP is attached as **Exhibit 22**. Documents referenced in this claim chart are attached hereto as **Exhibits 22A-D**. O2Micro took the photographs of the ASUSTeK F5AL-B2 attached hereto as **Exhibit 22A**, drew the schematic of the inverter circuit found in that product attached hereto as **Exhibit 22C**, and printed test data for the product attached here to as **Exhibit 22D**. **Exhibit 22B** is a publicly available datasheet of the MPS 1010B. Upon information and belief, MPS customers utilize MPS' inverter circuit reference design in substantially the same manner as

shown regarding ASUSTeK F5AL-B2 notebook containing the CCFL inverter circuit with MPS model number 1010BEP.

6.6 A claim chart demonstrating how independent claims 1 and 8 of the '382 patent apply to the LG 32BL9D 32" LCD television containing the CCFL inverter circuit with Microsemi model number LX1691a is attached as **Exhibit 23**. Documents referenced in this claim chart are attached hereto as **Exhibits 23A-D**. O2Micro took the photographs of the LG 32BL9D attached hereto as **Exhibit 23A**, drew the schematic of the inverter circuit found in that product attached hereto as **Exhibit 23C**, and printed test data for the product attached here to as **Exhibit 23D**. **Exhibit 22B** is a publicly available datasheet of the Microsemi LX1691. Upon information and belief, Microsemi customers utilize Microsemi's inverter circuit reference design in substantially the same manner as shown regarding the LG 32BL9D 32" LCD television containing the CCFL inverter circuit with Microsemi model number LX1691a.

6.7 A claim chart demonstrating how claim 7 of the '519 patent applies to the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model number MP1009 is attached as **Exhibit 24**. Documents referenced in this claim chart are attached hereto as **Exhibits 24, 27-30**. O2Micro took the photographs of the BenQ E2200HD attached hereto as **Exhibit 27**, drew the schematic of the inverter circuit found in that product attached hereto as **Exhibit 28**, and printed test data for the product attached here to as **Exhibit 29**. Upon information and belief, MPS customers utilize MPS' inverter circuit reference design in substantially the same manner as shown regarding the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model number MP1009.

6.9 A claim chart demonstrating how independent claim 1 of the '938 patent applies to the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model

number MP1009 is attached as **Exhibit 25**. Documents referenced in this claim chart are attached hereto as **Exhibits 25, 27-30**. Upon information and belief, MPS customers utilize MPS' inverter circuit reference design in substantially the same manner as shown regarding the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model number MP1009.

6.8 A claim chart demonstrating how independent claim 4 of the '035 patent applies to the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model number MP1009 is attached as **Exhibit 26**. Documents referenced in this claim chart are attached hereto as **Exhibits 26-30**. Upon information and belief, MPS customers utilize MPS' inverter circuit reference design in substantially the same manner as shown regarding the BenQ E2200HD LCD monitor containing the CCFL inverter circuit with MPS model number MP1009.

VII. SPECIFIC INSTANCES OF UNFAIR IMPORTATION AND SALE

7.1 Upon information and belief, Respondents' CCFL inverter circuits and products containing the same are sold for importation into the United States, imported into the United States or sold after importation into the United States.

7.2 Attached as **Exhibit 31** is a copy of a receipt reflecting the sale of a CCFL inverter circuit and ASUSTeK notebook computer in the United States. **Exhibit 14** includes photographs of the ASUSTeK notebook Model No. F5AL-B2. As can been seen in these photographs, the packaging for the ASUSTeK F5AL-B2 and the notebook itself are labeled "MADE IN CHINA" In addition, **Exhibit 14** includes photographs of the panel of the ASUSTeK F5AL-B2 notebook computer on which a CCFL inverter with MPS model No. 1010BEP, is mounted.

7.3 Attached as **Exhibit 32** is a copy of a receipt reflecting the sale of a LG 32BL9D 32" LCD television in the United States. **Exhibit 15** includes photographs of the packaging for the LG 32BL9D 32" LCD television and the television itself. As can been seen in these photographs, the packaging for the LG 32BL9D 32" LCD television and the television itself are labeled "MADE IN KOREA" and "Assembled in Mexico." In addition, **Exhibit 15** includes photographs of the board for the LG 32BL9D 32" LCD television showing the CCFL inverter circuit with Microsemi model number LX1691a.

7.4 Attached as **Exhibit 33** is a copy of a receipt reflecting the sale in the United States of a BenQ E2200HD Series LCD Monitor. **Exhibit 21** includes photographs of the packaging for the BenQ E2200HD Series LCD Monitor and the monitor itself. As can been seen in these photographs, the packaging for the BenQ E2200HD Series LCD Monitor and the monitor itself are labeled "MADE IN CHINA." In addition, **Exhibit 21** includes photographs of the board for the BenQ E2200HD Series LCD Monitor showing the CCFL inverter circuit with MPS model number MP1009.

VIII. CLASSIFICATION OF THE INFRINGING PRODUCTS UNDER THE HARMONIZED TARIFF SCHEDULE OF THE UNITED STATES

8.1 Upon information and belief, Respondents' infringing products may be classified under at least the following headings of the Harmonized Tariff Schedule of the United States: 8542.39.00; 8528.59.30.50; and 8528.72.72.50.

IX. LICENSEES

9.1 O2 Micro has licensed the '382, '519, '938 and '035 patents. **Confidential Exhibit 34** is a list of O2 Micro's licensees under the asserted patents.

X. THE DOMESTIC INDUSTRY

10.1. A domestic industry as defined by section 337(a)(2) and (3) exists in connection with O2 Micro's activities related to CCFL inverter products covered by the '382, '519, '938 and '035 patents. This industry includes O2 Micro's significant investment in plant, equipment, labor and capital in the United States relating to O2 Micros' activities, including the design, development, fabrication, manufacturing, testing of and engineering support for O2 Micro's entire product line of CCFL inverter products covered by the patents at issue.

A. O2 Micro's Exploitation of the Asserted Patent

10.2 For purposes of establishing domestic industry, O2 Micro states that it conducts activities in the United States relating to at least the OZ960 and OZ964 CCFL inverter circuits, which are covered by at least claim 1 of the '382 patent, and at least the OZ9RRA and OZ9936 CCFL inverter circuits, which are covered by at least claim 1 of the '519 patent, claim 1 of the '938 patent and claim 4 of the '035 patent. These four products are merely representative of O2 Micro's family of CCFL inverter products that utilize the patented inventions. These products practice the asserted claims when used by O2 Micro's domestic customers.

10.3 A claim chart applying claim 1 of the '382 patent to O2 Micro's OZ960 is attached as **Confidential Exhibit 35**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 35A**. This chart demonstrates O2 Micro's practice of the '382 patent by a CCFL inverter circuit with its OZ960.

10.4 A claim chart applying claim 1 of the '382 patent to O2 Micro's OZ964 is attached as **Confidential Exhibit 36**. Documents referenced in this claim chart are attached

hereto as **Confidential Exhibit 36A-B**. This chart demonstrates O2 Micro's practice of the '382 patent by a CCFL inverter circuit with its OZ964.

10.5 A claim chart applying claim 1 of the '519 patent to O2 Micro's OZ9RRA is attached as **Confidential Exhibit 37**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 37A**. This chart demonstrates O2 Micro's practice of the '519 patent by a CCFL inverter circuit with its OZ9RRA.

10.6 A claim chart applying claim 1 of the '519 patent to O2 Micro's OZ9936 is attached as **Confidential Exhibit 38**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 38A**. This chart demonstrates O2 Micro's practice of the '519 patent by a CCFL inverter circuit with its OZ9936.

10.7 A claim chart applying claim 1 of the '938 patent to O2 Micro's OZ9RRA is attached as **Confidential Exhibit 39**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 39A**. This chart demonstrates O2 Micro's practice of the '938 patent by a CCFL inverter circuit with its OZ9RRA.

10.8 A claim chart applying claim 1 of the '938 patent to O2 Micro's OZ9936 is attached as **Confidential Exhibit 40**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 40A**. This chart demonstrates O2 Micro's practice of the '938 patent by a CCFL inverter circuit with its OZ9936.

10.9 A claim chart applying claim 4 of the '035 patent to O2 Micro's OZ9RRA is attached as **Confidential Exhibit 41**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibit 41A**. This chart demonstrates O2 Micro's practice of the '035 patent by a CCFL inverter circuit with its OZ9RRA.

10.10 A claim chart applying claim 4 of the '035 patent to O2 Micro's OZ9936 is attached as **Confidential Exhibit 42**. Documents referenced in this claim chart are attached hereto as **Confidential Exhibits 42A**. This chart demonstrates O2 Micro's practice of the '035 patent by a CCFL inverter circuit with its OZ9936.

B. O2 Micro has Significant U.S. Investment in Plant Equipment, Labor and Capital

10.11 O2 Micro has made significant investments in plant, equipment, labor and capital in the United States relating to O2 Micro CCFL inverter circuits that practice the asserted patents, specifically the OZ960, OZ964, OZ9RRA and OZ9936 CCFL inverter circuits. Since their introductions, O2 Micro's sales of these products have been significant. *See* **Confidential Exhibit 43**. O2 Micro's activities in connection with the '382, '519, '938 and'035 patents, for purposes of the domestic industry requirement of Section 337, in this investigation occur in O2 Micro's facility in Santa Clara, California and at the fabrication facility in Texas utilized by O2 Micro[1].

10.12 O2 Micro has substantially invested in its facility in Santa Clara, California where the CCFL inverter products are designed, developed, tested and supported. **Confidential Exhibit 45** sets forth the square footage and value of O2 Micro's Santa Clara facility.

10.13 O2 Micro's significant investment also includes significant investment in equipment and other capital expenditures such as, salaries, software, creation of prototypes, improvements to the Santa Clara facility and other non-reoccurring engineering costs relating to O2 Micro's efforts associated the OZ960, OZ964, OZ9RRA and OZ9936 CCFL inverter circuits

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1 **Confidential Exhibit 44** is the Supply Agreement between O2 Micro and its fabrication partner.

that practice the '382, '519, '938 and'035 patents. These costs are reflected in **Confidential Exhibit 46**. In addition, O2 Micro has invested significant capital in the Texas fabrication facility used for the fabrication of the OZ964, OZ9RRA and OZ9936 CCFL inverter products. This investment is set forth in **Confidential Exhibit 47**.

10.14 O2 Micro has also invested significant resources of labor in its efforts associated with the OZ960, OZ964, OZ9RRA and OZ9936 CCFL inverter products. *See* **Confidential Exhibit 48**. This investment includes the man-hours spent in designing, developing, testing, and supporting the OZ960, OZ964, OZ9RRA and OZ9936 inverter products.

XI. RELATED LITIGATION

11.1 The foreign patents that are counterparts sharing the '382 patent specification, which is the subject of this Complaint, are the subject of litigation in the following actions:

- *O2Micro International Limited v. Beyond Innovation Technology Co., Ltd., & Samsung Electronics Co., Ltd.,* Taipei District Court, (92) Chih-tzu No. 21 and (95) Chih-tzu No. 38: O2 Micro sued Samsung and Beyond Innovation Technology for infringement of Taiwan Patent No. 152318. The litigations have been settled and the actions were dismissed.
- *O2Micro International Limited v. Monolithic Power Systems, Inc. & ASUSTeK Computer Inc.,* Taipei District Court, (93) Chih-tzu No. 33: O2 Micro sued MPS and ASUSTeK for infringement of Taiwan Patent No. 152318. This case has been sent to assessment intuition for an opinion on several matters including infringement and invalidity.
- *O2Micro International Limited v. CLEVO Co.,* Banciao District Court, (94) Chung-Chih-tsu No. 14: O2 Micro sued Clevo for infringement of Taiwan Patent No. 152318. The litigation has been settled and the action was dismissed.

11.2 The '519, '938 and'035 patents are the subject of the following litigation:

- *Monolithic Power Systems, Inc. v. O2 Micro International Limited,* C-08-4567 (N.D. Cal.): On October 1, 2008, MPS filed a complaint seeking a declaratory judgment of non-infringement and invalidity against O2 Micro of the '519, '938 and '035 patents and U.S. Patent No. 6,900,993. Although a complaint has been filed, this lawsuit has not yet been served on O2Micro.

11.3 Pursuant to Commission Rule 210.12(a)(5), there are no other court or agency litigation, foreign or domestic, involving the unfair acts or the subject matter of this Complaint.

XII. RELIEF REQUESTED

12.1 WHEREFORE, by reason of the foregoing, Complainant O2 Micro requests that the United States International Trade Commission:

(a) institute an immediate investigation pursuant to 19 U.S.C. § 1337(a)(1)(B)(i) and (b)(1) into the violations of that section based on Respondents' unlawful importation into the United States, sale for importation into the United States, and/or sale in the United States after importation of certain CCFL inverter Circuits and products containing the same that infringe one or more of the claims of U.S. Patent No. 7,417,382, U.S. Patent No. 6,856,519, U.S Patent No. 6,809,938 and U.S. Patent No. 7,120,035;

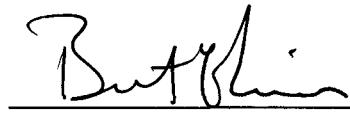
(b) issue orders pursuant to 19 U.S.C. § 1337(d), excluding from entry into the United States all imported Respondents' CCFL inverter circuits and all products, including notebook computers, LCD panels and LCD televisions, containing Respondents' infringing CCFL inverter circuits, that infringe one or more of the claims of U.S. Patent No. 7,417,382, U.S.

Patent No. 6,856,519, U.S Patent No. 6,809,938 and U.S. Patent No. 7,120,035;

(c) issue permanent orders pursuant to 19 U.S.C. § 1337(f) directing Respondents to cease and desist from importing, marketing, advertising, demonstrating, warehousing of inventory for distribution, sale and use of CCFL inverter circuits and products containing the same that infringe one or more claims of the patent at issue; and

(d) grant such other and further relief as the Commission deems appropriate and just under the law, based on the facts complained of herein and determined by the investigation.

Respectfully submitted,



Dated: December 15, 2008

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Counsel for Complainants
O2 Micro International Ltd. and
O2 Micro Inc.

VERIFICATION OF COMPLAINT

I, Yung-Lin Lin, declare, in accordance with 19 C.F.R. 210.4 and 210.12(a), under penalty of perjury, that the following statements are true:

1. I am the Executive Vice-President of Intelligent Lighting Group of O2 Micro, Inc., and I am duly authorized to sign this Complaint on behalf of all of the Complainants;

2. I have read the foregoing Complaint;

3. To the best of my knowledge, information, and belief, based upon reasonable inquiry, the foregoing Complaint is well-founded in fact and is warranted by existing law or by a non-frivolous argument for the extension, modification, or reversal of existing law, or the establishment of new law;

4. The allegations and other factual contentions have evidentiary support or are likely to have evidentiary support after a reasonable opportunity for further investigation or discovery; and

5. The foregoing Complaint is not being filed for an improper purpose, such as to harass or cause unnecessary delay or needless increase in the cost of litigation.

Executed this 15th day of December, 2008.

Yung-Lin Lin
Executive Vice-President of
Intelligent Lighting Group
O2 Micro, Inc.

Exhibit 12

FILED
IN CLERK'S OFFICE
U.S. DISTRICT COURT E.D.N.Y
★ AUG 07 2009 ★
BROOKLYN OFFICE

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF NEW YORK
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POWERTECH ASSOCIATION LLC,

Plaintiff,

- against -

O2 MICRO INTERNATIONAL LTD.; O2 MICRO INC.; TOSHIBA CORPORATION; TOSHIBA AMERICA, INC.; VIEWSONIC CORPORATION; SUMIDA CORPORATION; and SUMIDA AMERICA INC.,

Defendants.

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09 3446

JURY TRIAL DEMANDED

VITALIANO, J.

MANN. M.J.

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Powertech Association LLC files this Complaint and demand for jury trial seeking relief for patent infringement by the Defendants. Powertech Association LLC states and alleges the following:

THE PARTIES

1. Plaintiff Powertech Association LLC ("Powertech") is a limited liability company organized and existing under the laws of the State of Delaware.

2. On information and belief, Defendant O2 Micro International Ltd. is a corporation organized under the laws of the Cayman Islands with its principal place of business at The Grand Pavilion, West Bay Road, PO Box 32331 SMB, George Town, Grand Cayman, Cayman Islands, but doing business throughout this judicial district and around the world.

3. On information and belief, O2 Micro Inc. is a corporation organized and existing under the laws of California with its principal place of business at 3118 Patrick Henry Drive,

Santa Clara, CA 95054. On information and belief, Defendant O2 Micro Inc. is a wholly owned subsidiary of O2 Micro International Ltd.

4. On information and belief, Defendant Toshiba Corporation is a corporation organized under the laws of the Japan with its principal place of business at 1-1, Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan, but doing business throughout this judicial district and around the world.

5. On information and belief, Toshiba America, Inc. is a corporation organized and existing under the laws of Delaware with its principal place of business at 1251 Avenue of the Americas, Suite 4110, New York, NY 10020. On information and belief, Defendant Toshiba America, Inc. is a wholly owned subsidiary of Toshiba Corporation.

6. On information and belief, Defendant ViewSonic Corporation is a corporation organized under the laws of the California with its principal place of business at 381 Brea Canyon Road, Walnut, CA 91789-0708, but doing business throughout this judicial district and around the world.

7. On information and belief, Defendant Sumida Corporation is a corporation organized under the laws of the Japan with its principal place of business at 1-6-6, Yaesu, Chuo-ku, Tokyo 103-8589, Japan, but doing business throughout this judicial district and around the world.

8. On information and belief, Sumida America Inc. is a corporation organized and existing under the laws of Delaware with its principal place of business at 1251 N. Plum Grove Road, Suite 150, Schaumburg, IL 60173. On information and belief, Defendant Sumida America Inc. is a wholly owned subsidiary of Sumida Corporation.

JURISDICTION AND VENUE

9. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 1 *et seq*. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

10. The Court has personal jurisdiction over Defendants O2 Micro International Ltd. and O2 Micro Inc. (collectively, "O2 Micro"); Toshiba Corporation and Toshiba America, Inc. (collectively, "Toshiba"); ViewSonic Corporation ("ViewSonic"); and Sumida Corporation and Sumida America Inc. (collectively, "Sumida") because they have committed acts of patent infringement in this judicial district. Defendants have placed infringing products into the stream of commerce by shipping those products into this judicial district (and other judicial districts) or knowing that such products would be shipped into this judicial district (and other judicial districts).

11. Venue is proper in this judicial district under 28 U.S.C. §§ 1391(b) and (c) and 1400(b) because, among other reasons, Defendants are subject to personal jurisdiction in this judicial district and have committed acts of infringement in this judicial district.

FIRST CLAIM FOR RELIEF
INFRINGEMENT OF US PATENT NO. 6,979,959

12. Powertech restates and realleges paragraphs 1-11 of this Complaint.

13. On December 27, 2005, United States Patent No. 6,979,959 ("the '959 patent") entitled "Apparatus and method for striking a fluorescent lamp" was duly and legally issued by the United States Patent and Trademark Office. Powertech is the owner of the '959 patent by assignment of all right, title, and interest. A true and correct copy of the '959 patent is attached as Exhibit A.

14. O2 Micro has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '959 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, integrated circuits used in CCFL drivers including but not limited to inverter controllers, such as OZ964, OZ9RR, OZ9925, OZ9936, OZ9910 and OZ9938 product families.

15. Toshiba has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '959 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits, including but not limited to the Toshiba Satellite U405D-S2902 laptops, which include, e.g., a panel identified by part numbers LP133WX (TL) (N3), LGA9252MS83JH0626B1, and 13392C8237641 222D, and an inverter circuit board identified by part number IV10117/T-LF which includes an OZ9910.

16. ViewSonic has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '959 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits, including but not limited to the ViewSonic N1930w HDTV/PC monitor combinations, which include, e.g., a panel identified by part numbers M190MWW1-401, I0S0MBM1904932610266, and MD19441066KS1KSV93Q0155, and an inverter circuit board identified by part number JT198MSP 2202140300P Rev 1.00, which includes an OZ9938.

17. Sumida has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '959 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, inverter circuit boards incorporating O2 Micro's integrated circuits, including but not limited to the Sumida IV10117/T-LF.

18. Powertech has been damaged and has suffered irreparable injury due to Defendants' unlawful infringement of the '959 patent, and Powertech will continue to suffer irreparable harm and damages unless Defendants' activities are enjoined.

19. On information and belief, O2 Micro has knowledge of the '959 patent because O2 Micro routinely monitors patents issued by its competitors, one of which is Microsemi Corporation, the original assignee of the '959 patent.

SECOND CLAIM FOR RELIEF
INFRINGEMENT OF US PATENT NO. 7,279,852

20. Powertech restates and realleges paragraphs 1-11 of this Complaint.

21. On October 9, 2007, United States Patent No. 7,279,852 ("the '852 patent") entitled "Apparatus and method for striking a fluorescent lamp" was duly and legally issued by the United States Patent and Trademark Office. Powertech is the owner of the '852 patent by assignment of all right, title, and interest. A true and correct copy of the '852 patent is attached as Exhibit B.

22. O2 Micro has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '852 patent under 35 U.S.C. § 271, by making, using, selling and/or offering to sell within and/or importing into the United States, including this judicial district, integrated circuits used in CCFL drivers

including but not limited to inverter controllers, such as OZ964, OZ9RR, OZ9925, OZ9936, OZ9910 and OZ9938 product families.

23. Toshiba has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '852 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits, including but not limited to the Toshiba Satellite U405D-S2902 laptop, which include, e.g., a panel identified by part numbers LP133WX (TL) (N3), LGA9252MS83JH0626B1, and 13392C8237641 222D, and an inverter circuit board identified by part number IV10117/T-LF which includes an OZ9910.

24. ViewSonic has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '852 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits, including but not limited to the ViewSonic N1930w HDTV/PC monitor combinations, which include, e.g., a panel identified by part numbers M190MWW1-401, I0S0MBM1904932610266, and MD19441066KS1KSV93Q0155, and an inverter circuit board identified by part number JT198MSP 2202140300P Rev 1.00, which includes an OZ9938.

25. Sumida has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '852 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, inverter circuit boards incorporating O2 Micro's integrated circuits, including but not limited to the Sumida IV10117/T-LF.

26. Powertech has been damaged and has suffered irreparable injury due to Defendants' unlawful infringement of the '852 patent, and Powertech will continue to suffer irreparable harm and damages unless Defendants' activities are enjoined.

27. On information and belief, O2 Micro has knowledge of the '852 patent because O2 Micro routinely monitors patents issued by its competitors, one of which is Microsemi Corporation, the original assignee of the '852 patent.

THIRD CLAIM FOR RELIEF
INFRINGEMENT OF US PATENT NO. 7,411,360

28. Powertech restates and realleges paragraphs 1-11 of this Complaint.

29. On August 12, 2008, United States Patent No. 7,411,360 ("the '360 patent") entitled "Apparatus and method for striking a fluorescent lamp" was duly and legally issued by the United States Patent and Trademark Office. Powertech is the owner of the '360 patent by assignment of all right, title, and interest. A true and correct copy of the '360 patent is attached as Exhibit C.

30. O2 Micro has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '360 patent under 35 U.S.C. § 271, by making, using, selling and/or offering to sell within and/or importing into the United States, including this judicial district, integrated circuits used in CCFL drivers including but not limited to inverter controllers, such as OZ964, OZ9RR, OZ9925, OZ9936, OZ9910 and OZ9938 product families.

31. Toshiba has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '360 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits,

including but not limited to the Toshiba Satellite U405D-S2902 laptop, which include, e.g., a panel identified by part numbers LP133WX (TL) (N3), LGA9252MS83JH0626B1, and 13392C8237641 222D, and an inverter circuit board identified by part number IV10117/T-LF which includes an OZ9910.

32. ViewSonic has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '360 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, electronics incorporating O2 Micro's integrated circuits, including but not limited to the ViewSonic N1930w HDTV/PC monitor combinations, which include, e.g., a panel identified by part numbers M190MWW1-401, I0S0MBM1904932610266, and MD19441066KS1KSV93Q0155, and an inverter circuit board identified by part number JT198MSP 2202140300P Rev 1.00, which includes an OZ9938.

33. Sumida has infringed and continues to infringe directly and/or indirectly, literally and/or under the doctrine of equivalents, one or more claims of the '360 patent under 35 U.S.C. § 271, by making, using, selling, and/or offering to sell within and/or importing into the United States, including this judicial district, inverter circuit boards incorporating O2 Micro's integrated circuits, including but not limited to the Sumida IV10117/T-LF.

34. Powertech has been damaged and has suffered irreparable injury due to Defendants' unlawful infringement of the '360 patent, and Powertech will continue to suffer irreparable harm and damages unless Defendants' activities are enjoined.

35. On information and belief, O2 Micro has knowledge of the '360 patent because O2 Micro routinely monitors patents issued by its competitors, one of which is Microsemi Corporation, the original assignee of the '360 patent.

PRAYER FOR RELIEF

WHEREFORE, Powertech respectfully requests that this Court enter judgment and provide relief as follows:

(1) That Defendants have infringed the '959 patent, the '852 patent, and the '360 patent;

(2) That Defendants and their officers, agents, servants, employees, and all persons in active concert or participation with them directly or indirectly, be enjoined from infringing the '959 patent, the '852 patent, and the '360 patent;

(3) That Defendants be ordered to account for and pay to Powertech the damages resulting from Defendants' infringement of the '959 patent, the '852 patent, and the '360 patent, together with interest and costs, and all other damages permitted by 35 U.S.C. § 284, including enhanced damages up to three times the amount of damages found or measured;

(4) That this action be adjudged an exception case and Powertech be awarded its attorneys' fees, expenses, and costs in this action pursuant to 35 U.S.C. § 285; and

(5) That Powertech be awarded such other equitable or legal relief as this Court deems just and proper under the circumstances.

JURY TRIAL DEMAND

Powertech demands a trial by jury on all issues so triable.

Dated: August 7, 2009

FISH & RICHARDSON P.C.

By: _____

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Lewis Hudnell
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New York, NY 10022-4611
Ph: 212-765-5070
Fax: 212-765-5070

Attorneys for Plaintiff
Powertech Association LLC

Exhibit 13
to
Exhibit 15

Redacted In Their Entirety